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... years ahead

MODEL 7500
PROGRAMMABLE
DIGITAL MULTIMETER

INSTRUMENT
CENTER

(1978) $2995.00

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3rd Edition

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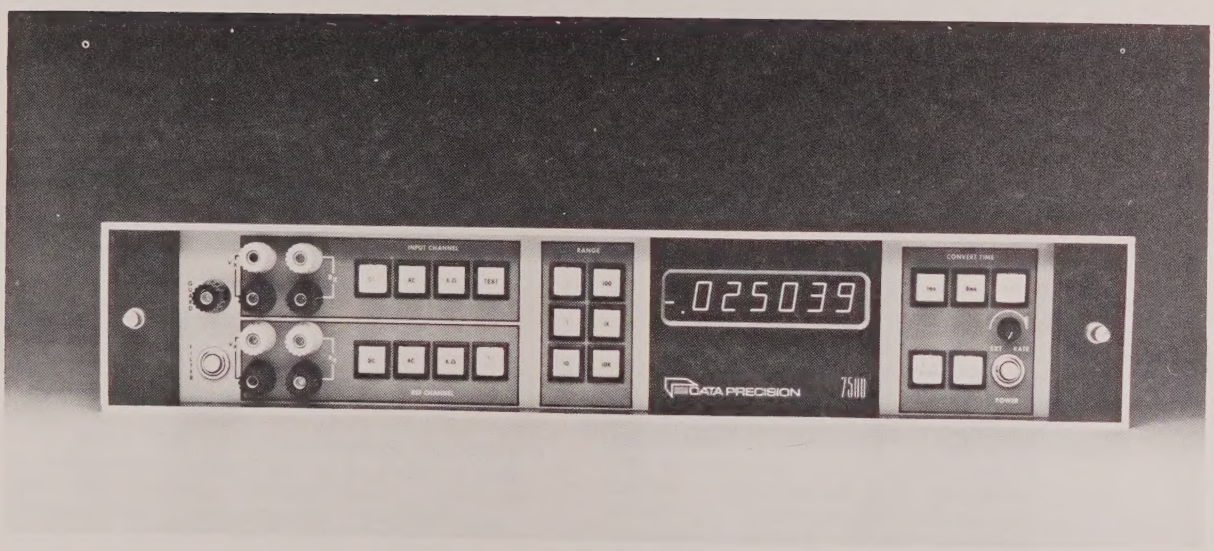

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1 INTRODUCTION

1.1 GENERAL

Model 7500 Programmable Digital Multimeter (Frontispiece) is a 5-1/2 digit, high speed, local and remote programmable system - compatible instrument. It provides the user with capability for measuring dc volts, ac volts, or resistance with respect to a precision internally developed reference standard, or with respect to externally connected dc volts, ac volts, or resistance references. Moreover, the user may select the reference independently of the measurand, obtaining whatever ratio measurement is required.

1.2 FEATURES

a. High Speed.

Model 7500 may be programmed to complete a measurement conversion in as short a time as 1 millisecond. Through local (front) or remote (rear) panel control, the user may select a complete measurement time of 1, 8, or 64 milliseconds (for 60 Hz installations), or 1.2, 10, or 80 milliseconds (for 50 Hz installations).

b. High Resolution/High Stability.

The 5-1/2 digit conversion provides a resolution of 1 part in 200000 for in-range measurements on any one of 5 decade range scales (6 for resistance measurements). The least significant digit provides a meaningful 1 microvolt and 1 milliohm resolution, supported by reliable accuracy and stability performance specifications. The quadraphasic™ conversion technique provides an autozeroing operation and each conversion is preceded by an autozeroing compensation. No zero adjustment is needed, and none is provided.

c. Computer - Compatible Programming.

All Model 7500 DMM functions may be controlled by externally programmed signals (except power application). Moreover, provision is made for control of function groups (Ranges, Signal Conditioning units, Measurement Times) so that controls for one or more groups may be restricted to local (front-panel) operation. Interfacing with particular bus configurations is accomplished through microcomputer programming installed within the Model 7500.

d. Modular Construction.

Model 7500 system architecture utilizes a standard rack & panel mounting configuration in which functional modules are replaceable plug-in assemblies. Options, providing for ac voltage measurements, resistance measurements, reference ac and dc voltage ratios and resistance ratios, are easily added at any time as plug-in assemblies for which all "mother-board" interconnections are already pre-wired. In addition, the interface options are instrumented through two such plug-in assemblies. Power for the options is provided in the Basic instrument.

e. Built-In Test.

Precision references (1 volt and 10 volts) may be internally connected by local or remote program control to test Model 7500 operation.

1.3 QUADRAPHASIC™ CONVERSION

Model 7500 DMM utilizes Data Precision's proprietary 4-phase A/D conversion technique by which high-speed, high accuracy, high stability measurement is obtained. The four phases are:

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Phase 1: A minimum time interval, depending upon the selected conversion time, during which internal instrumentation offsets are zeroed out of the conversion circuitry.

Phase 2: Integration of the conditioned measurand, charging an integrating capacitor for a fixed time interval to a level proportional to the conditioned measurand.

Phase 3: Integration of the conditioned reference at a fast rate, discharging the integrating capacitor until within 1% of the full scale value.

Phase 4: Integration of the conditioned reference at a slow rate, continuing the discharge of the integrating capacitor and providing a vernier count for the measured value.

Figure 1-1 illustrates the quadra-phasic cycle operation showing the charge-discharge cycle of the integrating capacitor for a measurement of an in-range negative dc voltage input. Note the introduction of pauses to permit switching transients to settle. Note, also, that the count intervals are determined by the selected measurement conversion time.

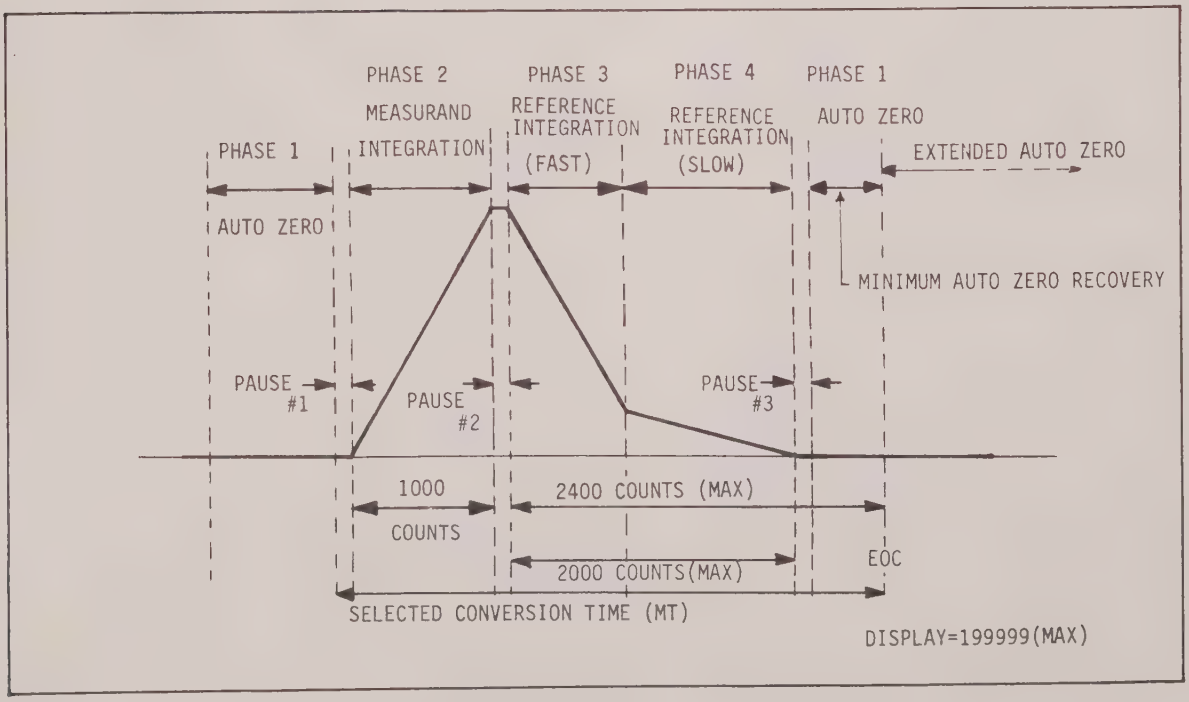

Figure 1-1. System Timing Waveforms

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1.4 SPECIFICATIONS

1.4.1 Absolute Maximum Voltage Ratings, unless otherwise specified. (Sea level to 10,000 feet,70% relative humidity or less.)

(a) Common Mode:

Guard to Chassis - ±1000V peak DC to 120Hz
Guard to Input Low - 150V peak
Input High to Chassis - 200V peak DC to 120Hz

(b) Normal Mode:

Input High to Input Low - ±1415V peak to 10KHz derate to ±360V peak at 100 KHz

1.4.2 DC Volts (Internal DC Reference).

Range	Full Scale Reading	L.S.D. Resolution	Input Impedance
+.100000	+.199999	1uV	1000 Meg.
±1.00000	±1.99999	10uV	1000 Meg.
±10.0000	±19.9999	100uV	1000 Meg.
±100.000	±199.999	1mV	10 Meg.
±1000.00	±1000.00*	10mV	10 Meg.

*Maximum voltage limitation of all DC ranges ±1000 volts.

1.4.2.1 Accuracy

(a) 64 ms measurement time
24 hours, 23°C ±1°C

+0.100000 Range - ±0.004% input ±0.003% range ±1 l.s.d.
All Other Ranges - ±0.004% input ±0.001% range ±1 l.s.d.

6 months, 23°C ±5°C

+0.100000 Range - ±0.008% input ±0.003% range ±1 l.s.d.
All Other Ranges - ±0.007% input ±0.001% range ±1 l.s.d.

Add ±0.00001% reading/1 Volt

(b) 8 ms measurement time

+0.100000 range - Add ±0.002% range
All Other Ranges - Add ±0.001% range

(c) 1 ms measurement time

+0.100000 Range - Add ±0.002% input ±0.008% range
All Other Ranges - Add ±0.002% input ±0.004% range

1.4.2.2 Temperature Coefficient (0° to 50°C).

+0.100000 Range - (±0.001% input ±.0005% range)/°C
All Other Ranges - (±.0008% input ±0.0002% range)/°C

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1.4.2.3 Settling Time.

(a) Filter Out:

0.5 ms to rated accuracy from full scale step
5 ms to rated accuracy from overload

(b) Filter In:

500 ms to rated accuracy from full scale step or overload

1.4.2.4 Input Current (Kickback) Maximum.

±10pA DC ±10pA peak AC

1.4.2.5 Common Mode Rejection.

At DC, 140dB with 1000Ω unbalanced source impedance
At 60Hz*, 120dB with 1000Ω source impedance @ 64 ms measurement time
At 60Hz*, 60dB with 1000Ω source impedance @ 8 ms and 1 ms measurement time

*50 Hz in Model 7500E

1.4.2.6 Capacity from Guard to Chassis: 2500 pf

1.4.2.7 Ranging: Manual, Automatic, or Remote

1.4.2.8 Normal Mode Rejection.

(a) Filter Out:

60dB at 60Hz 64 ms measurement time

(b) Filter In:

100dB at 60Hz 64 ms measurement time
40dB at 60Hz 8 ms and 1 ms measurement time

1.4.3 External DC Reference Input (Signal/DC ratio input).

Standard DC reference input conditioning permits DCV/DCV ratio and with appropriate options in the signal channel ACV/DCV and ohm/DCV ratio measurements.

External Reference Voltage Range: ±1V to ±11V*
Input Resistance: 100 k ohms*
Overvoltage Protection: ±100V peak
Common Mode Voltage (with respect to signal channel low): ±10V
CMRR: 96dB
Settling Time: 0.5 ms to rated accuracy from full scale step; 500 ms to within ±0.01% of range from overload

*(Other values available as factory installed options.)

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1.4.4 DC/DC Ratio (4 Quadrant, 4 Terminal).

Signal Input Range	Full Scale Reading*	DC Reference Input
±.100000	±.199999	±1V to ±11V
±1.00000	±1.99999	±1V to ±11V
±10.0000	±19.9999	±1V to ±11V
±100.000	±199.999	±1V to ±11V
±1000 0	±1999.99**	±1V to ±11V

*Display reads 10 X ratio of signal voltage to reference voltage.
**Maximum signal input voltage limited to 1000 volts.

1.4.4.1 Accuracy: 6 months 23°C ±5°C

(a) 64 ms measurement time
±0.100000 range $\frac{\pm(0.008\% \text{ signal input } \pm 0.003\% \text{ range } \pm 1 \text{ l.s.d.}) \times 10}{\text{Reference Input Voltage}}$

Other ranges: $\frac{\pm(0.007\% \text{ signal input } \pm 0.001\% \text{ range } \pm 1 \text{ l.s.d.}) \times 10}{\text{Reference Input Voltage}}$

(b) 8 ms and 1 ms measurement times
Add terms indicated under DC volts

1.4.4.2 Temperature Coefficient (0°C to +50°C):

(Same as DC/Internal Reference) $\times \frac{10}{\text{Reference Input Voltage}}$

1.4.4.3 Settling Time:

(a) Filter Out:

0.5 msec. to rated accuracy from full scale range
5 msec. to rated accuracy from overload

(b) Filter In:

500 msec. to rated accuracy from full scale step

1.4.4.4 Ranging: Manual, Automatic, or Remote

1.4.5 AC Volts (Option AC1):

(a) Sensing and Calibration
Full wave average, calibrated in rms of sinewave

Range	Full Scale Reading	Resolution
.100000	.199999	1uV
1.00000	1.99999	10uV
10.0000	19.9999	100uV
100.000	199.999	1mV
1000.00*	1000.00*	10mV

*See maximum voltage limitation below.

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1.4.5.1 Input Impedance (all ranges): 1 Megohm shunted by 250pf (front and rear panel inputs in parallel)

1.4.5.2 Accuracy (6 months, 23°C ±5°C): 64 ms measurement time interpolate linearly between specified points.

(a) 1 Volt - 100V Ranges:

40Hz:	±0.1% input ±.01% range
100Hz to 1kHz:	±0.05% input ±.01% range
10kHz:	±0.2% input ±.01% range
30Hz and 100kHz:	±1% input ±0.05% range

(b) 0.1 Volt Range:

40Hz:	±0.1% input ±0.1% range
100Hz to 1kHz:	±0.05% input ±0.1% range
10kHz:	±0.2% input ±0.1% range
30Hz and 100kHz:	±1% input ±0.5% range

1.4.5.3 Temperature Coefficient (0°C to 50°C):

(a) 1 Volt - 100V Ranges:

30Hz - 1kHz:	(±0.005% input ±0.001% range)/°C
1kHz - 10kHz:	[(±0.005 X frequency in kHz)% input ±0.001% range]/°C
10kHz - 100kHz:	(±0.05% input ±0.001% range)/°C

(b) 0.1 Volt Range:

30Hz - 1kHz:	(±0.005% input ±0.01% range)/°C
1kHz - 10kHz:	[(±0.005 X frequency in kHz)% input ±0.01% range]/°C
10kHz - 100kHz:	(±0.05% input ±0.02% range)/°C

1.4.5.4 Maximum Input Voltage:

Sinewave:

30Hz to 1kHz:	1000 VRMS
1kHz to 10kHz:	decrease linearly to 700 VRMS at 10kHz
above 10kHz:	decrease linearly to 250 VRMS at 100kHz

DC superimposed on AC shall not exceed ±600V

1.4.5.5 Settling Time: 360 msec. to rated accuracy ±0.05% of range for full scale step input.

1.4.5.6 Ranging: Manual, Automatic, or Remote

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1.4.6 AC (Option AC2):

Sensing: True RMS, AC coupled

Range	Full Scale Reading	Resolution
.100000	.199999	1uV
1.00000	1.99999	10uV
10.0000	19.9999	100uV
100.000	199.999	1mV
1000.00*	1000.00*	10mV

*See maximum voltage limitation below.

1.4.6.1 Input Impedance (all ranges): 1 Megohm shunted by 250pf (front and rear panel inputs in parallel)

1.4.6.2 Accuracy (6 months, 23°C ±5°C): 64 ms measurement time interpolate linearly between specified points.

(a) 1 Volt - 1000 Volt Ranges:

Sinewave (.01 X Range V in RMS 2 X Range)

50Hz:	±.25% input ±.05% range
100Hz - 1kHz:	±.15% input ±.05% range
10kHz:	±.4% input ±.1% range
100kHz:	±3% input ±.5% range

(b) .1 Volt Range:

Sinewave (0.1 X Range V in RMS 2 X Range)

50Hz:	±.25% input ±.5% range
100Hz - 1kHz:	±.15% input ±.5% range
10kHz:	±.4% input ±1% range
100kHz:	±3% input ±5% range

1.4.6.3 Temperature Coefficient (0°C to 50°C):

(a) 1 Volt - 1000 Volt Ranges:

50Hz - 1kHz:	(±.01% input ±.015% range)/°C
100kHz:	(±.1% input ±.05% range)/°C

(b) .1 Volt Range:

50Hz - 1kHz:	(±.01% input ±.15% range)/°C
100kHz:	(±.1% input ±.5% range)/°C

1.4.6.4 Maximum Input Voltage:

Sinewave

50Hz - 1kHz:	1000 VRMS
10kHz:	700 VRMS
100kHz:	250 VRMS

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1.4.6.5 Repetitive Non-Sinewave (1000V range and overload of other ranges):

Maximum input slew rate < 65V/us	1425V peak
65 V/us < Maximum input slew rate < 225V/us	1000V peak
225V/us < Maximum input slew rate < 1000V/us	400V peak

DC Superimposed on AC shall not exceed ±600 Volts

1.4.6.6 Settling Time: 500 msec. to final reading ±.1% of range for a full scale step input

1.4.6.7 Crest Factor: 7 minimum at V in RMS = 1 X Range

1.4.6.8 Peak Input: (±10 X Range) Volts

1.4.7 AC/DC Ratio (with AC1 or AC2 Options):

Signal input ranges and full scale reading same as AC volts except 1000V range reads ratio to 1999.99 subject to signal voltage vs. frequency limits. Display reads 10 X ratio with standard ±1V to ±11V external DC references.

1.4.7.1 Accuracy: 6 months 23°C ±5°C

(Same as corresponding AC volts range accuracy) $\times \frac{10}{\text{Reference Input Voltage}}$

1.4.7.2 Temperature Coefficient (0°C to +50°C):

(Same as corresponding AC volts range TC) $\times \frac{10}{\text{Reference Input Voltage}}$

1.4.7.3 Settling Time: Same as AC Volts

All other signal channel parameters same as AC Volts
All other reference channel parameters per external DC reference

1.4.8 OHMS (Option Ohms 1)

Range	Full Scale Reading	Resolution	Maximum Test Current
.10000 k ohms	.199999 k ohms	1 milliohm	1mA
1.0000 k ohms	1.99999 k ohms	10 milliohms	1mA
10.000 k ohms	19.9999 k ohms	100 milliohms	100uA
100.00 k ohms	199.999 k ohms	1 ohm	10uA
1000.0 k ohms	1999.99 k ohms	10 ohms	1uA
10000. k ohms	19999.9 k ohms	100 ohms	.1uA

1.4.8.1 Configuration: True four-wire

1.4.8.2 Maximum Open Circuit Voltage: 5V

1.4.8.3 Maximum Fault Input: 250 VRMS or DC, 360V peak

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1.4.8.4 Accuracy (6 months, 23°C, ±5°C): 64 ms measurement time

0.1 k ohm range:	±0.01% input ±0.004% range ±1 l.s.d.
1 kohm/10 kohm/100 kohm ranges:	±0.01% input ±0.002% range ±1 l.s.d.
1000 kohm range:	±0.02% input ±0.002% range ±1 l.s.d.
10000 kohm range:	±0.15% input ±0.002% range ±1 l.s.d.

1.4.8.5 Temperature Coefficient (0°C to 50°C):

0.1 k ohm range:	(±0.002% input ±0.001% range)/°C
1 kohm/10 kohm/100 kohm ranges:	(±0.002% input ±0.0004% range)/°C
1000 kohm range:	(±0.005% input ±0.0004% range)/°C
10000 kohm range:	(±0.02% input ±0.005% range)/°C

1.4.8.6 Settling Time (To within rated accuracy ±0.005% of range):

(a) Filter Out:

(0.5 + 0.3 X Resistance in kohms) ms

(b) Filter In:

(0.5 + 6 X Resistance in Megohms) seconds

1.4.8.7 Ranging: Manual, Automatic, or Remote

1.4.9 OHMS/DC Ratio (with Ohms 1 Option):

Signal input ranges and full scale readings same as ohms. Display reads 10 X ratio with standard ±1V to ±11V external DC reference.

1.4.9.1 Accuracy: 6 months, 23°C, ±5C

$$\text{(Same as corresponding ohms range accuracy)} \times \frac{10}{\text{Reference Input Voltage}}$$

1.4.9.2 Temperature Coefficient (0°C to +50°C):

$$\text{(Same as corresponding ohms range TC)} \times \frac{10}{\text{Reference Input Voltage}}$$

All other signal channel parameters same as ohms. All other reference channel parameters same as external DC reference.

1.4.10 External AC Reference (Options Ref. AC01-05):

Sensing and Calibration
Full wave average, calibrated in RMS of a sinewave

Ref. AC Option #	Ref. Range	Min. Ref. Input (Rated Accuracy)	Max. Ref. Input (Rated Accuracy)	Display Ratio Multiplier
01	0.1	0.01	0.11	0.1X
02	1.0	0.1	1.1	1X
03	10.	1.0	11.0	10X
04	100.	10.	110	100X
05	250	100	260	1000X

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1.4.10.1 Maximum Voltage Ratings:

(a) 260 VRMS (all ranges) relative to signal channel low. Reference channel low is connected to signal channel low when AC Reference is selected.peak plus superimposed DC not to exceed 400V.

(b) AC Input Impedance - 1 Megohm shunted by 250pf

1.4.10.2 Signal/AC Ratio Accuracy

$$\frac{\left(\begin{array}{l}\text{Applicable signal channel accuracy} \\ \text{+ applicable AC reference accuracy}\end{array}\right) \times \text{(Display ratio multiplier)}}{\text{(AC Reference Input Voltage)}}$$

1.4.10.3 AC Reference Accuracy: (6 months, 23°C, ±5°C) (Interpolate linearly between frequencies.)

	AC Ref. Freq.	AC Ref. Accuracy
(a) Option 01	40Hz:	±0.2% input
	100Hz - 1kHz:	±0.15% input
	10kHz:	±0.3% input
	30Hz and 100kHz:	±1.5% input
(b) Option 02-05	40Hz:	±0.1% input
	100Hz - 1kHz:	±0.06% input
	10kHz:	±0.2% input
	30Hz and 100kHz:	±1% input

1.4.10.4 AC Reference Ratio Temperature Coefficient:

$$\text{(Applicable signal channel TC + AC reference TC)} \times \frac{\text{(Display Ratio Multiplier)}}{\text{(AC Reference Input Volt)}}$$

1.4.10.5 AC Reference TC (0°C to +50°C):

(a) Option 01	30Hz - 1kHz:	±0.015% input/°C
	1kHz - 10kHz:	±(0.009% + .006 X freq. in kHz)% input/°C
	10kHz - 100kHz:	±0.07% input/°C
(b) Option 02-05	30Hz - 1kHz:	±0.006% input/°C
	1kHz - 10kHz:	±(0.006 X freq. in kHz)% input/°C
	10kHz - 100kHz:	±0.06% input/°C

1.4.10.6 Settling Time: 360 msec. to rated accuracy ±0.05% of range from full scale step.

1.4.11 External Reference kohms (Options Ref. Ohms 02-06):

Ref. Ohms Option #	Range	Min. Input	Max. Input	Test Current	Display Ratio Multiplier
02	1 kohm	1.1 kohm	1.1 kohm	1mA	1X
03	10 kohm	1.0 kohm	11 kohm	100uA	10X
04	100 kohm	10 kohm	110 kohm	10uA	100X
05	1000 kohm	100 kohm	1.1 Megohm	1uA	1000X
06	10000 kohm	1 Megohm	11 Megohm	0.1uA	10000X

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1.4.11.1 Configuration:

Full four-wire capability for independent resistors. May be used in two-wire configuration. Usable with the main channel ohms current driving both signal and reference resistors simultaneously for measurements near unity ratio on ranges other than the nominal range. With test current disconnected and reference ohm selected, the sensing terminals provide a true differential high impedance 1 Volt range external DC reference capability.

1.4.11.2 Maximum Test Voltage: 5V

1.4.11.3 Input Overvoltage Protection: 200 VRMS or DC

1.4.11.4 Signal/Ohms Ratio Accuracy:

$$\frac{\left(\begin{array}{l}\text{Applicable signal channel accuracy +}\\ \text{applicable reference ohms accuracy}\end{array}\right) \text{X (Display Ratio Multiplier)}}{\text{(Reference Input, k Ohms)}}$$

1.4.11.5 External Reference Ohms Accuracy (6 months, 23°C, ±5°C)

Ref. Ohms	
Option 02	±0.013% input
Option 03	±0.015% input
Option 04	±0.02% input
Option 05	±0.025% input
Option 06	±0.15% input

1.4.11.6 Temperature Coefficient (0°C to +50°C, referred to signal channel)

Option 02, 03	±0.0025% input/°C
Option 04	±0.005% input/°C
Option 05	±0.009% input/°C
Option 06	±0.025% input/°C

1.4.11.7 Settling Time (to within rated accuracy ±0.005% of range):

(0.5 + 0.3 X Resistance in kohms) ms

1.4.11.8 Options

The basic 7500 unit provides for the easy addition of plug-in modules to expand its capabilities. Single, 44-pin P.C. connector slots are prewired to accommodate each of the following generic groups of options:

Slot A1	Reference ohms and/or special reference DC signal conditioning
Slot A2	Ohms (current source) options
Slot A3	Reference AC signal conditioning options
Slot A4	AC signal conditioning options

Two dual 44-pin P.C. connector slots (A10, A11) are prewired to the digital input, output and internal status lines for interface use. Output connections from these slots is by ribbon cable to connectors mounted on a removable sub-panel attached to the rear panel for easy field installation as interface requirements change. Standard options occupying one or both of these slots include the following:

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Basic parallel optoisolated I/O options
IEEE STD-488-1975 Microprocessor-controlled General Purpose Interface Bus option
RS-232/TTY microprocessor controlled interface option

1.4.12 INTERFACE AND APPLICATIONS DATA

1.4.12.1 Digital Control Units

The 7500 DMM can be remotely operated by the following CMOS/DTL/TTL - compatible signals: (Low is < +0.4V, high is > +3.5V input impedance 10k to ground standard, other termination resistance values and pull up termination optional).

(a) External Trigger: A positive pulse 1 microsecond or more wide initiates a measurement cycle if the unit is armed and the external triggering is selected. A high DC level initiates continual measurements at the maximum rate possible for the selected measurement time.

(b) $\overline{\text{Arm}}$: A low DC level or open circuit on this input continuously enables external triggering. A high level inhibits remote triggering. A pulsed low of 1 microsecond minimum that is removed before completion of the next measurement cycle arms a single measurement.

(c) Remote Programming Bus: A group of 6 bus lines and 4 function strobe lines which permit complete remote programming of 4 signal channel functions, 4 reference channel functions, 6 ranges, autoranging, 3 measurement times, filter in, filter out. All programming functions are internally latched and buffered for rapid and convenient computer control. To select a function, the appropriate code is applied to the six (6) bus lines at least 0.5 μ seconds before the function strobe pulse. The required strobe pulse duration is 2 μ seconds and bus data may change 0.5 μ seconds after the strobe pulse end. The controller may change any programmable functions at this 3 microsecond per change rate without waiting for the completion of the preceding change. Completion of all changes is indicated by the low to high transition of the Programming Busy flag output.

(d) Local and Remote Lockout: A group of 5 lines which can be connected to Logic One prevent actuation of programming functions from the front panel when only remote operation is desired or to prevent remote operation when only front panel control is desired.

Local Lockout - Disables all front panel controls except power and trigger rate unless one or more remote lockout lines are activated. (REMPROG SEL)

Signal Remote Lockout - Disables remote program control of the 4 signal channel functions and enables front panel control of those functions. (GX)

Reference Remote Lockout - Disables remote program control and enables front panel control of the 4 reference functions. (GRC)

Range Remote Lockout - Disables remote program control and enables front panel control of the 6 ranges and autorange. (GRA)

Measurement Time Lockout - Disables remote program control and enables front panel control of the 3 measurement times and filter in, filter out. (GMT)

1.4.12.2 Digital Outputs

All digital outputs are DTL/TTL/CMOS compatible with a fanout of 2 standard TTL loads. Logic one > +2.4V. Logic zero < +0.4V sinking 3.2mA. The outputs are:

(a) Measurement Data: Five full BCD 8-4-2-1 coded lines, 1 line most significant digit, and 1 line polarity. (Positive polarity = logic one.)

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(b) $\overline{\text{Overload}}$: 1 line (Logic zero = overload)

(c) Range: 6 lines (logic zero = range not in use; logic one = range in use)

(d) Converting: End of conversion is signalled by the high to low transition of this line. When ranges are changed in autorange, this line remains high until a conversion is completed on the correct range.

(e) Integrating Signal: A flag which indicates that the analog input signal is being measured. After the high to low transition of this line, the analog input signal may be removed or changed without affecting the measurement result (unless autorange has been selected and the result is out-of-range). The reference input in ratio measurements must remain stable for the remainder of the conversion, until CONVERTING GOES LOW.

(f) $\overline{\text{Programming Busy}}$: A flag which indicates that changes of function are in progress which prevent making measurements. Multiple changes of functions may be made during the active (zero) interval of this flag and it times out after the last change. The user may then trigger new measurements, making suitable allowance for analog settling time depending on the function range and input where required.

1.4.13 POWER SUPPLY OUTPUT

An auxilliary regulated power output of +5VDC at 1A is available at the rear connector. (The available current is reduced when certain interface options are installed.)

1.4.14 OPERATING SPEEDS

(a) Conversion Time: 1, 8 or 64 millisec. nominal manual or remotely selected. (Model 7500E)
1.2, 10, or 80 millisec for Model 7500E.

(b) Conversion Rate: Internal: Adjustable from front panel 2 to 15 conversions per second. Externally triggered: Zero to 15, 125, 1000 conversions per second nominal depending on selected conversion time; zero to 12.5,100, 830 conversions per sec. for Model 7500E.

(c) Range-Changing Time: 40 milliseconds

(d) Auto-Ranging Time: DC filter out - conversion time + 60 milliseconds per range change. AC, ohms, DC filter in - conversion time + 360 milliseconds per range change. Down-ranging skips any intermediate ranges. Up-range goes direct to the highest range, measures, then down-ranges direct to the correct range if required.

1.4.15 POWER REQUIREMENTS

36 Watts, maximum at 105-125 VAC or 210-250 VAC selected by rear panel switch, 47-500Hz,for unit with AC, ohms, ref. AC and ref. ohms options installed. A 7500 optimized for normal mode rejection in 50Hz operation is available as an option, (MODEL 7500E). Power supply voltage ranges of 90-110VAC are available as Option S32.

1.4.16 ENVIRONMENT

(a) Temperature Range: 0°C to +50°C operating
-25°C to +70°C storage

(b) Humidity: 70% RH maximum, operable to 95% RH noncondensing with derating of peak input and common mode voltages.

1.4.17 PHYSICAL CHARACTERISTICS

Panel Size: 3-1/2" high x 19" wide (8.89 cm x 48.26 cm)
Chassis Size: 17" wide x 17" from front panel inner surface (43.18 cm x 43.18 cm)
Overall Size: 3-1/2" x 19" x 18" (8.89 cm x 48.26 cm x 45.72 cm)
Weight: 26 pounds (11.8Kg)

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1.5 ORDERING GUIDE

1.5.1 Shipping Configuration

a. The Model 7500 DMM is shipped complete with installed modules, including those for the ordered optional signal conditioners and interfaces. Table 1-1 translates the order code in terms of the option assemblies comprising installed for each designated option.

b. Two extender cards are included with each Basic 7500. Mating connectors for all rear panel connectors are attached, as well as a protective cover for front panel input binding posts.

c. Instruction manual, certificate of conformance, and final factory test data sheets are packed with each instrument.

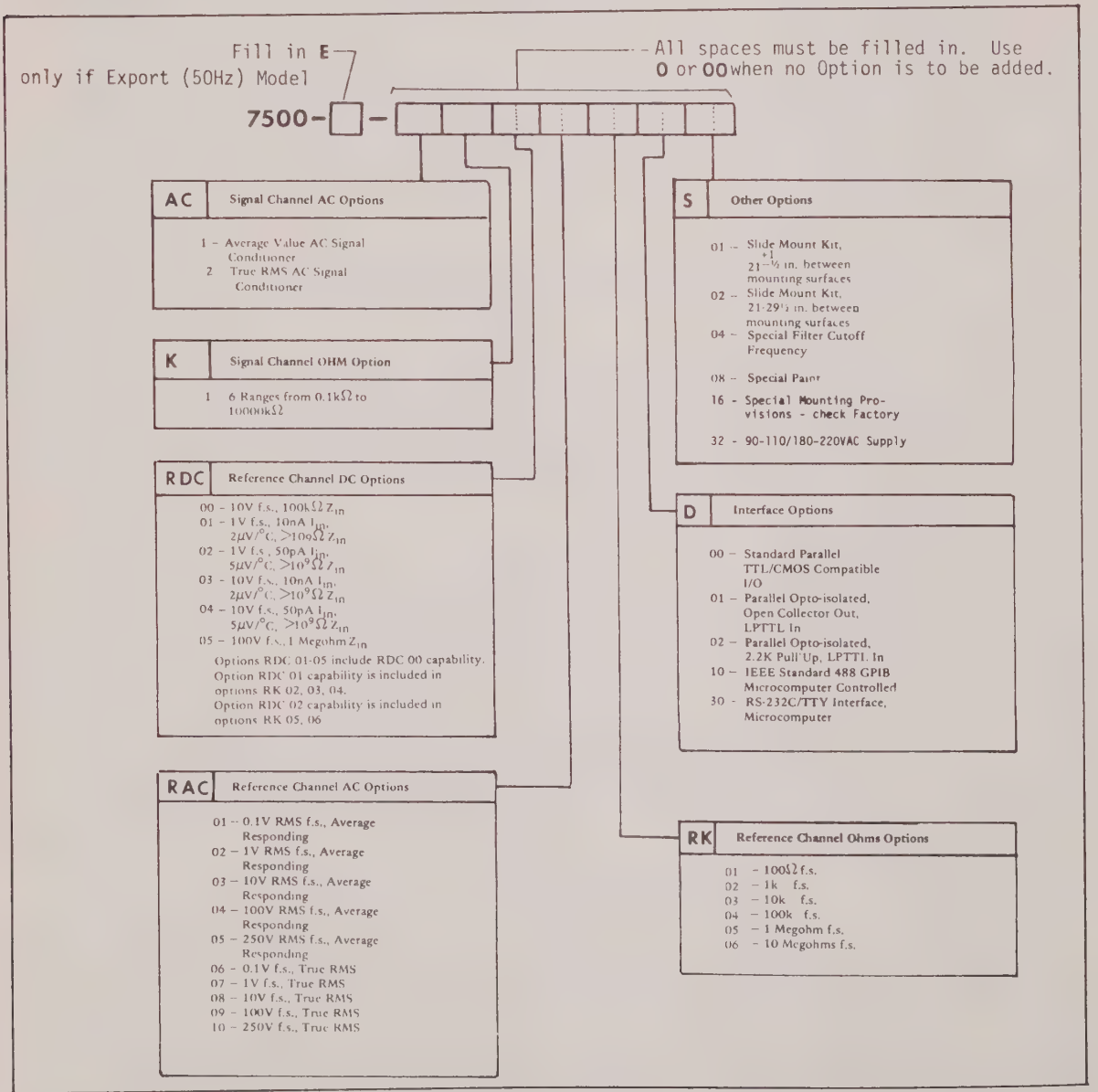
Fill in E only if Export (50Hz) Model
All spaces must be filled in. Use 0 or 00 when no Option is to be added.
7500-□-
AC Signal Channel AC Options
1 - Average Value AC Signal Conditioner
2 True RMS AC Signal Conditioner
K Signal Channel OHM Option
1 6 Ranges from 0.1kΩ to 10000kΩ
RDC Reference Channel DC Options
00 - 10V f.s., 100kΩ Z_{in}
01 - 1V f.s., 10nA I_{in}, 2μV/°C, >10⁹Ω Z_{in}
02 - 1V f.s., 50pA I_{in}, 5μV/°C, >10⁹Ω Z_{in}
03 - 10V f.s., 10nA I_{in}, 2μV/°C, >10⁹Ω Z_{in}
04 - 10V f.s., 50pA I_{in}, 5μV/°C, >10⁹Ω Z_{in}
05 - 100V f.s., 1 Megohm Z_{in}
Options RDC 01-05 include RDC 00 capability.
Option RDC 01 capability is included in options RK 02, 03, 04.
Option RDC 02 capability is included in options RK 05, 06
RAC Reference Channel AC Options
01 - 0.1V RMS f.s., Average Responding
02 - 1V RMS f.s., Average Responding
03 - 10V RMS f.s., Average Responding
04 - 100V RMS f.s., Average Responding
05 - 250V RMS f.s., Average Responding
06 - 0.1V f.s., True RMS
07 - 1V f.s., True RMS
08 - 10V f.s., True RMS
09 - 100V f.s., True RMS
10 - 250V f.s., True RMS
S Other Options
01 - Slide Mount Kit, 21 +1 −½ in. between mounting surfaces
02 - Slide Mount Kit, 21-29½ in. between mounting surfaces
04 - Special Filter Cutoff Frequency
08 - Special Paint
16 - Special Mounting Provisions - check Factory
32 - 90-110/180-220VAC Supply
D Interface Options
00 - Standard Parallel TTL/CMOS Compatible I/O
01 - Parallel Opto-isolated, Open Collector Out, LPTTL In
02 - Parallel Opto-isolated, 2.2K Pull Up, LPTTL In
10 - IEEE Standard 488 GPIB Microcomputer Controlled
30 - RS-232C/TTY Interface, Microcomputer
RK Reference Channel Ohms Options
01 - 100Ω f.s.
02 - 1k f.s.
03 - 10k f.s.
04 - 100k f.s.
05 - 1 Megohm f.s.
06 - 10 Megohms f.s.

Table 1-1

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FIELD INSTALLATION OF OPTIONS - MODEL 7500

OPTION	TEST DATA SHEET	INSTALLATION PROCEDURE	PARTS LIST	ASSY	PROCEDURE / REF. DRAWINGS
AC1	52-2006	52-1002	PL50-1009	057-1007	PLUG-IN MODULE IN SLOT XA9. REPLACE PUSHBUTTON CAP. CHECK CALIBRATION.
AC2	52-2008	52-1002	PL50-1093	057-1093	PLUG-IN MODULE IN SLOT XA9. REPLACE PUSHBUTTON CAP. CHECK CALIBRATION.
K1	52-2007	52-1003	PL50-1010	057-1010	PLUG-IN MODULE IN SLOT XA8. REPLACE PUSHBUTTON CAP. CHECK CALIBRATION.
ROC Ø Ø (7500 STD)	52-2000	N/A	N/A	N/A	IF REMOVING ANOTHER ROC, RK OR RAC WITHOUT REPLACEMENT, REPLACE PUSHBUTTON CAP WITH BLANK CAP & INSTALL 8 JUMPERS ON MOTHER BD. PER TABLE ON 057-1080 SHEET 2.
ROC01	52-2002	52-1004	PL50-1073	057-1072	
ROC02	52-2003	52-1004	PL50-1074	057-1072	
ROC03	52-2004	52-1004	PL50-1076	057-1075	
ROC04	52-2005	52-1004	PL50-1077	057-1075	
ROC05	52-2006	52-1004	PL50-1079	057-1079	PLUG-IN MODULE IN SLOT XA1, REPLACE BLANK PUSHBUTTON CAP WITH
RKØ1	52-2017	52-1006	PL50-1104	057-1029	MARKED CAP. REMOVE GREEN OR ORANGE JUMPERS AS
RKØ2	52-2018	52-1006	PL50-1037	057-1029	APPLICABLE AND INSTALL RED JUMPERS IF REQ'D PER TABLE
RKØ3	52-2019	52-1006	PL50-1038	057-1029	ON 057-1020, SHEET 2. CHECK CALIBRATION.
RKØ4	52-2020	52-1006	PL50-1039	057-1029	
RKØ5	52-2021	52-1006	PL50-1040	057-1029	
RKØ6	52-2022	52-1006	PL50-1041	057-1029	
RACØ1	52-2009	52-1005	PL50-1033	057-1028	
RACØ2	52-2010	52-1005	PL50-1034	057-1028	
RACØ3	52-2010	52-1005	PL50-1035	057-1028	PLUG IN MODULE IN SLOT XA9. REPLACE BLANK PUSHBUTTON CAP WITH
RACØ4	52-2010	52-1005	PL50-1036	057-1028	MARKED CAP. REMOVE RED OR ORANGE JUMPERS AS
RACØ5	52-2011	52-1005	PL50-1061	057-1028	APPLICABLE AND INSTALL GREEN JUMPERS IF REQ'D PER TABLE
RACØ6	52-2012	52-1005	PL50-1090	057-1089	ON 057-1020, SHEET 2. CHECK CALIBRATION.
RACØ7	52-2013	52-1005	PL50-1091	057-1089	
RACØ8	52-2014	52-1005	PL50-1092	057-1089	
RACØ9	52-2015	52-1005	PL50-1093	057-1089	
RAC10	52-2016	52-1005	PL50-1094	057-1089	
DØ Ø (7500 STD)					STANDARD. NONE REQUIRED.
DØ1		057-1071	PL50-1071	057-1071	
DØ2		057-1071	PL50-1078	057-1071	
D10		A55-1038	PL50-1088	057-1088	
D30			PL50-1098	057-1098	
3Ø1		057-1097	PL50-1097	057-1097	
3Ø2		057-1097	PL50-1065	057-1097	

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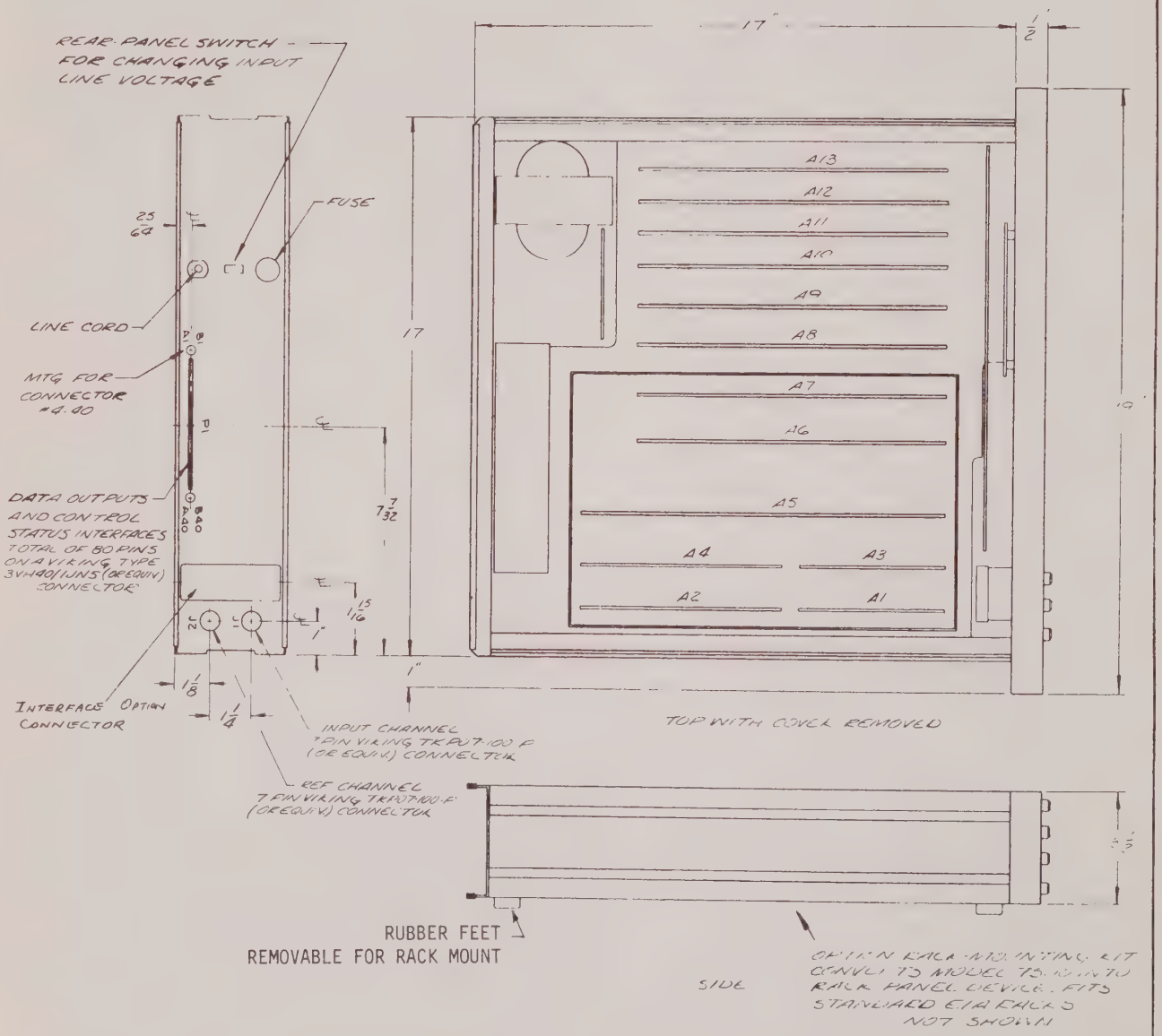

Figure 1-2. Model 7500 DMM Outline and Mounting Dimensions

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2
LOCAL OPERATION

2.1 GENERAL - SCOPE OF CHAPTER

Chapter 2 contains instructions for operating Model 7500 DMM under program control of the front-panel operating controls. The chapter also includes instructions for front-panel connections when making DCV, ACV, Kilohms, and Ratio measurements, as well as step-by-step procedures in carrying out these measurements. Instructions for remote programming control and for remote transmission of measurement data are contained in Chapter 3.

2.2 FRONT PANEL CONTROLS & INDICATORS

2.2.1 Organization.

The front panel elements of Model 7500 DMM are organized into functional groups that reflect the general operating design of the multimeter. Essentially, the measurement process is one of a ratio calculation in which the input measurand (numerator) and input reference (denominator) may be selected independently by the user according to the measuring code desired. In addition, the numerator may also be derived from the precision internal reference for a TEST measurement.

2.2.2 Control Function.

a. Figure 2-1 is a line drawing of the Model 7500 DMM front panel, and Table 2-1 contains a brief description of the items indexed in the illustration.

b. Figure 2-1 also shows a line drawing of the rear panel, and Table 2-1 includes descriptions of the items indexed there.

2.3 POWER CONNECTIONS

a. Model 7500 is shipped with the rear panel select switch in position for the anticipated power source at the receiving point, either 115V or 230V ac.

CAUTION

Verify that power-select switch on the Model 7500 rear panel is in proper position for the source available. (Figure 2-1)

b. Connect 3-wire cord (2 active, 1 ground) to the correct power source.

c. Turn on POWER and allow 1 hour for equipment to warm-up before making measurements, if rated accuracy is required.

2.4 SIGNAL CONNECTIONS

WARNING

OBSERVE APPLICABLE VOLTAGE RATINGS FOR ALL CONNECTIONS. (Para 2.4) Failure to comply with voltage ratings may result in equipment damage or hazardous conditions.

The Model 7500 DMM rear input connections are internally connected in parallel with the binding posts at the front panel. Before using one set of input connections (front or rear), always check to see that incompatible connections have not been made to the other set of inputs. If connections are to be made to rear input connector, install plastic protector (provided with basic unit) over front-panel binding posts.

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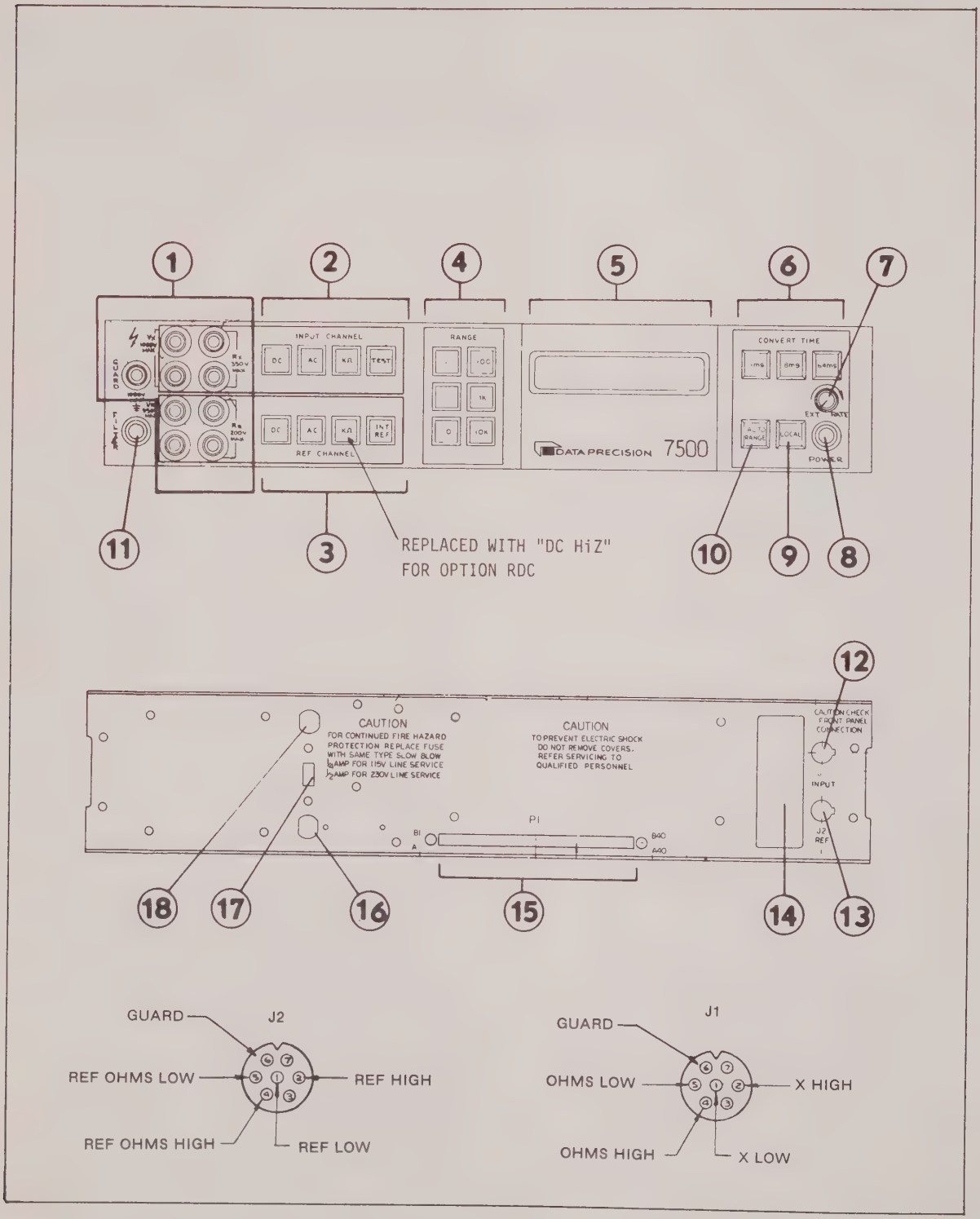

Figure 2-1. Model 7500 DMM Front and Rear Panel displays, controls, and indicators.

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Table 2-1

MODEL 7500 CONTROLS & INDICATORS

REF ITEM NO.	MARKING DESIGNATION or DESCRIPTION	FUNCTIONAL DESCRIPTION
1.	Vx HI & LO	5-way binding posts; input terminals for DC & AC Measurands and Kilohms sensing
	Rx HI & LO	5-way binding posts; Kilohms current drive terminals
	Vr HI & LO	5-way binding posts; input terminals for DC & AC References and Ref Kilohms sensing
	Rr HI & LO	5-way binding posts; Ref Kilohms current drive terminals
	GUARD	5-way binding post
2.	INPUT CHANNEL	Three lighted pushbuttons (DC, AC, and KΩ) that connect the Vx signal to selected input signal-conditioning circuitry, and one pushbutton (TEST) that connects a precision dc voltage signal to the input channel. The four buttons are electrically interlocked so that selecting a new one releases the others.
3.	REF CHANNEL	Three lighted pushbuttons (DC, AC, and KΩ) that connect the Vr signal to selected reference signal conditioning circuitry, and one pushbutton (INT REF) that connects a precision internal reference signal to the reference channel. The four buttons are electrically interlocked so that selecting a new one releases the others.
4.	RANGE	Six lighted pushbuttons (.1, 1, 10, 100, 1K, 10K) that set-up appropriate scaling circuitry so that the nominal range value is that shown on the pushbutton face. The pushbuttons are interlocked so that selecting a new one releases the others, including AUTO. RANGE 10K is effective only in Kilohms measurement.
5.	Display	Polarity sign (+,-), decimal point and 6 decimal digits (MSD is "1" or "0") displaying value of Vx with respect to Vr as each has been conditioned by the selected signal conditioning circuitry. Digits are 7-segment planar gas discharge.
6.	CONVERT TIME	Three lighted pushbuttons (1ms, 8ms, and 64ms) that set up appropriate circuitry for 1msec, 8msec, or 64msec conversion times of the input signal. The pushbuttons are interlocked so that selecting a new one releases the others.

(See Figure 2-1 for Reference Item No.)

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Table 2-1 (Continued)

REF ITEM NO.	MARKING DESIGNATION or DESCRIPTION	FUNCTIONAL DESCRIPTION
7.	EXT RATE	Potentiometer for trigger rate control. In extreme CCW detent position, trigger control is transferred to the rear panel remote connection. When rotated clockwise away from detent position, conversions are internally triggered from 2 to 15 per second.
8.	POWER	Push-push switch. Applies AC line power to Model 7500 DMM power supply circuits.
9.	LOCAL	Lighted push-push switch; when LOCAL is selected (light on), front panel controls are effective. When off, front panel controls are ineffective, except for those enabled by rear panel wiring connections, POWER and EXT RATE control.
10.	AUTO RANGE	Lighted push switch; selects auto ranging mode of operations. The range scale set up by the ranging circuitry when in auto range automatically positions the decimal point and controls the range scale selection light indicator in the range switches, item 4. Auto is deselected when a specific RANGE is selected locally or remotely.
11.	FILTER	Push-push switch; inserts built-in filter in Vx input signal path when in DCV or Kohms or TEST signal conditioning.
12.	J1 INPUT	5-prong connector, paralleling Vx HI Vx LO, Rx HI, Rx LO, and GUARD of front panel.
13.	J2 REF	5-prong connector, paralleling Vr HI, Vr LO, Rr HI, and Rr LO of front panel.
14.	Cut Out	Mounting area for interface connectors
15.	PC-Board Terminals	Mother-board connections for remote control, status, and data signals (2 x 40)
16.	Fuse	Holder and 1/4 Amp (115V) or 1/2 Amp 230V) slow blow fuse
17.	Switch	Slide switch for 115V or 230V power line selection (100V or 200V, Option S32)
18.	Line Cord	3-wire line cord for power sourcing.

* Measurement times of 1.2msec, 10msec, and 80msec are effective for Model 7500 E DMM, designed to be operated from 50 Hz ac sourcing.

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2.4.1 Absolute Maximum Voltages.

Model 7500 DMM is designed to measure voltages up to 1000 volts dc; 1000 VRMS at frequencies up to 1 KHz, derated to 250 VRMS at 100 KHz. These are limiting values of the potential difference between HI and LO of Vx. In addition, Model 7500 DMM may be operated with voltages of 150V peak between GUARD and LO, and 1000V peak (dc to 120 Hz) between GUARD and chassis, subject to an absolute maximum voltage limit of 2000 volts peak between chassis and Vx HI.

2.4.2 Voltage Measurement Connections.

Connect the measurand high and low to Model 7500 DMM as shown in Figure 2-2. Keep voltage potentials between terminals within the limits defined in para 2.4.1 above. Connect the GUARD to the source LO if possible. As alternates, but less desirable for common mode rejection, GUARD may be connected to the source ground or to the Vx LO terminal. Always connect GUARD when making measurements. Jumpers between Vx and Rx HI and between Vx and Rx LO may be left in place or removed when making voltage measurements.

2.4.3 Resistance Measurement Connections.

a. For 2-wire measurements, jumper Rx HI to Vx HI and to one end of the resistor to be measured; jumper Rx LO to Vx LO and to guard and to the other end of the resistor to be measured.

b. For 4-wire resistance measurements, remove jumpers; connect sourcing current from Rx HI and LO binding posts, and connect Vx HI and LO to unknown resistance as shown in Figure 2-3. Jumper the GUARD to Rx LO. Figure 2-4 illustrates a connection to be used when accurate resistance measurements are to be made in a noisy environment.

2.4.4 Ratio Measurements.

Connect the numerator inputs to the measurand terminals (Vx and Vr) as shown for the appropriate measurement in figures 2-2, 2-3, and 2-4. Connect the denominator inputs to the reference terminals (Rx and Rr) in the same way as for the appropriate numerator input illustration. Connect the GUARD as shown only for the numerator inputs.

2.5 PRE-OPERATION CHECK (POWER ON PER PARA 2.3)

a. Place LOCAL pushbutton in position for LOCAL control (light is on).

b. Operate INPUT CHANNEL TEST pushbutton.

c. Operate REF CHANNEL INT REF pushbutton.

d. Operate RANGE 1 pushbutton.

e. Operate CONVERT TIME 64ms pushbutton.

f. Adjust trigger control to mid-range position.

g. Read display. A value of $1.00000 \pm (.00006 + .0001\,\Delta^{\circ}C)(\Delta^{\circ}C = {}^{\circ}C - 23^{\circ}C)$ indicates an acceptable operable performance.

2.6 INTERPRETING THE DISPLAY

a. The decimal point is automatically positioned in the display so that all readings of voltage or resistance with internal reference are made directly in the units shown for the selected signal conditioning. The displayed value of Ratio may need to be interpreted for decimal point location depending upon the external reference range in use. Thus, +1.97565 in DCV measurement mode indicates that Vx HI is 1.97565 dc volts more positive than the LO

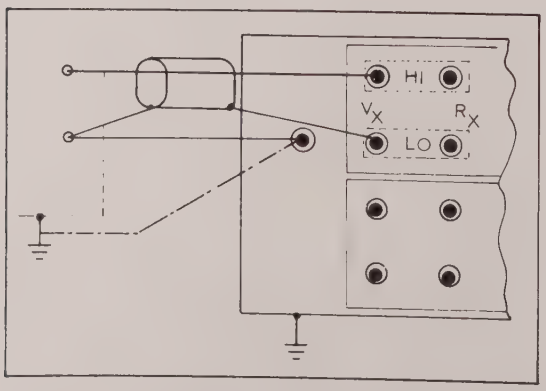

Figure 2-2. Connections for Voltage Measurements.

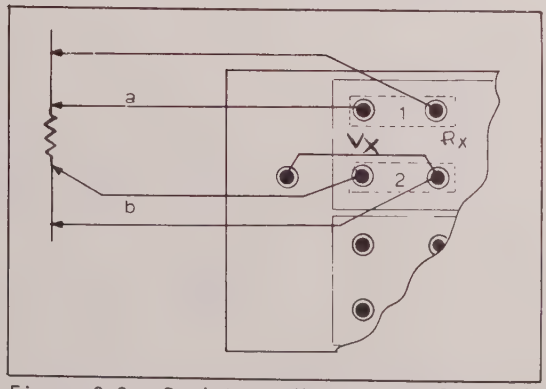

Figure 2-3. Resistance Measurement Connections. Jumpers 1 and 2 are removed for 4-Wire Connection.

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terminal, while a display of -197.565 in the same signal conditioning mode indicates that Vx HI is 197.565 dc volts less positive than the LO terminal. In the first instance, the decimal point location has been set by the selection of the RANGE 1 scale, while in the second instance, the decimal point location corresponds to a RANGE 100 selection.

b. A display of +01.9756 indicates a value of +1.9756 volts on a RANGE 10 scale. The 100% overrage capability of the Model 7500 (on all ranges except RANGE 1K for voltage) allows for a maximum reading of +1.99999 on the RANGE 1 scale, and a display value of +01.9756 indicates that a greater resolution is possible by shifting to RANGE 1. Note, however, that a display of +2.54760 is beyond display limits of the RANGE 1 scale. If RANGE 1 had been chosen, the display would present an out-of-range indication in which only the decimal point and the polarity sign remain lighted.

c. The RANGE 10K scale is effective only for KΩ measurements and electrically locked out otherwise. Operation of RANGE 10K pushbutton selects RANGE 1K in a voltage measurement mode. However, the 10K selection is "stored" so that a subsequent selection of Kilohms measurement causes the RANGE 10K to be selected. Thus, range may be selected before function.

2.7 MAKING DCV MEASUREMENTS

a. Operate INPUT CHANNEL DCV pushbutton.

b. Operate REF CHANNEL INT REF pushbutton.

c. Connect dc voltage signal source as described in paragraph 2.4.2.

d. Operate appropriate RANGE pushbutton for anticipated value, or operate AUTO RANGE pushbutton.

e. Operate appropriate CONVERSION TIME pushbutton. Select 64ms under normal circumstances. See Chapter 3 for discussion of the other selections.

f. Operate FILTER pushbutton to select filter when signal to be measured may have a high normal mode noise content, or when the source impedance is high and common mode noise is a problem.

g. Adjust trigger control for appropriate internally controlled conversion rate between 2 and 15 per second.

h. Read display directly in dc volts.

2.8 MAKING ACV MEASUREMENTS

a. Operate INPUT CHANNEL ACV pushbutton.

b. Operate REF CHANNEL INT REF pushbutton.

c. Connect input signal as described in paragraph 2.4.2.

d. Operate appropriate RANGE pushbutton or AUTO RANGE.

e. Operate appropriate CONVERSION TIME pushbutton, normally 64ms.

f. FILTER does not affect operation when ACV signal conditioning is selected.

g. Adjust trigger control for appropriate internally controlled rate of 2 to 15 conversions per second.

h. Read value directly on display. Display value is the rms value of a sine wave whose average full-wave rectified value equals the average value of the full-wave rectified input.

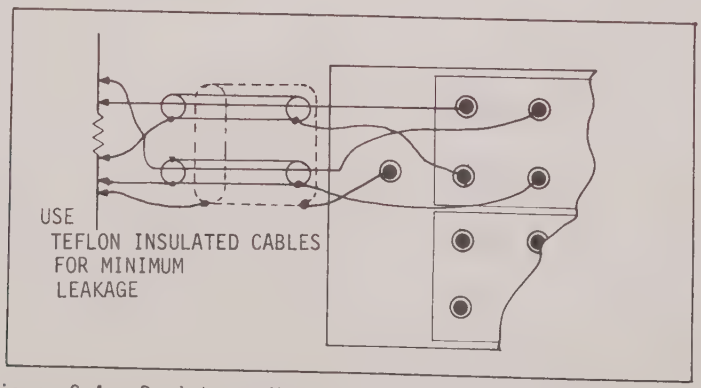

Figure 2-4. Resistance Measurement in noisy environment.

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2.9 MAKING RESISTANCE MEASUREMENTS

a. Connect the Model 7500 to the resistance 2- or 4-wire configuration as described in paragraph 2.5.2.

b. Operate CHANNEL INPUT KΩ pushbutton.

c. Operate REF INPUT INT REF pushbutton.

d. Operate appropriate RANGE pushbutton or AUTO RANGE pushbutton.

e. Operate CONVERSION TIME 64ms pushbutton.

f. Operate FILTER if additional noise rejection is desired.

g. Read display directly in kilohms.

2.10 MAKING RATIO MEASUREMENTS

a. Operate the appropriate INPUT CHANNEL and REF CHANNEL pushbuttons.

b. Connect the INPUT CHANNEL and REF CHANNEL inputs as described in para 2.4.2 (voltage) or 2.4.3 (resistance). Observe limitations on input and common mode voltages.

c. Operate the appropriate RANGE pushbutton or AUTO RANGE pushbutton.

d. Operate CONVERSION TIME pushbutton (normally 64ms).

Table 2-2

DISPLAY ADJUSTMENT

FACTORS TO BE USED FOR RATIO MEASUREMENTS

REF CHANNEL SELECTED SIGNAL CONDITIONING	OPTION INSTALLED	DIVIDE DISPLAYED VALUE BY FACTOR BELOW TO OBTAIN TRUE RATIO
INT REF	NA	1
DCV	NA	10
ACV	REF AC 01 06	0.1
ACV	REF AC 02 07	1
ACV	REF AC 03 08	10
ACV	REF AC 04 09	100
ACV	REF AC 05 10	1000
KΩ	REF OHMS 01	0.1
KΩ	REF OHMS 02	1
KΩ	REF OHMS 03	10
KΩ	REF OHMS 04	100
KΩ	REF OHMS 05	1000
KΩ	REF OHMS 06	10000
KΩ (when dc voltage is connected to Vr HI and LO)	REF OHMS 02-06 01	1 0.1

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3 REMOTE OPERATION

3.1 GENERAL

3.1.1 Basic, Remote Control Connector.

All Model 7500 DMM units provide a basic capability for remote programming of its measuring functions through a standard 2 x 40 pin pc-board connector. Command signals transmitted through this connector:

(1) select the conditioning circuitry for INPUT CHANNEL (measurand),

(2) select the conditioning circuit for the REF CHANNEL (reference),

(3) select the CONVERT time for the conversion cycle,

(4) connect and disconnect the filter when not in AC measuring mode, and

(5) select a fixed range or AUTO RANGE.

The remote control inputs may also control arming and trigger the conversion cycle. (Power can be turned ON or OFF only at the front panel.) As indicated previously, the programming functions may be exercised by both front and rear panel inputs, and, by optional wired connections of the Remote Control inputs, groups of functions may be reserved for front or rear panel input only. Program selections made remotely are indicated by lights on the front panel. Status signals indicating conversion in progress, programming busy, and integration of measurand are provided.

3.1.2 Remote Programming Options & Chapter Scope.

Model 7500 DMM architecture allocates two assembly modules, A10 and A11, on which to implement supplementary remote programming interfaces. Such interface modules provide the necessary protocols for specified applications, and each is described in a supplement to this chapter when that option is installed. In general, three main types of interface programming means are available. They are:

(1) Basic: CMOS/DTL/TTL - compatible control and status signals, available as part of the Basic Model 7500 DMM standard instrument. These inputs are also operable by contact closure.

(2) Opto-isolated: control and status signals in the same parallel format as the standard rear panel signals;

(3) Micro-processor formatting: control and status signals in accordance with the specified data bus requirements. (For example, IEEE STD-488-1975, and RS-232/TTY.)

3.2 BASIC REMOTE PROGRAMMING

3.2.1 Terminal Connections.

In order to utilize the Basic 7500 remote programming and output capability, the dual 40-pin connector (DP P/N 25-300002)*

* Viking #3VH40/1JN5 or equivalent

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should be wired as shown in figure 3-1. The control signals and data outputs identified in the illustration, have the following specifications and performance characteristics.

3.2.2 Digital Control Signals. (Signal names in capital letters.)

a. General: CMOS/DTL/TTL - compatible (0V < "0" < 0.8V; 5.5V > "1" > 3.5V). Input impedance 27 kohms to ground.

b. TRIGGER: A positive pulse, ≥1 μsec wide, initiates a measurement cycle if the Model 7500 is "armed" and if external triggering is enabled by the EXT-RATE switch. Continuous high level on the trigger results in repeated measurements at maximum rate possible when external triggering is effective.

c. $\overline{\text{ARM}}$: A low dc level (or open circuit) continuously enables external triggering. A high level inhibits triggering. If the $\overline{\text{ARM}}$ line is raised to a high level before the end of a conversion, that measurement is completed and held (thus arming a single measurement).

d. Remote Programming Bus (RP1, RP2, RP3, RP4, RP5, and RP6) and Strobes (STROBE X, STROBE REF, STROBE MT, and STROBE RANGE): The levels on the 6 bus lines are decoded when strobed to establish the selected programming function. Table 3-1 lists the bus encoding for each programmable function. The measurement time strobe, STROBE MT, simultaneously activates the filter selection with the measurement time selection. The bus lines must be set to the required levels at least 0.5 microseconds before the high level is applied to the strobe line. The strobe pulse must be at least 2 microseconds wide, and the bus lines may be changed not sooner than 0.5 microseconds after the end of strobe pulse.

e. Local and Remote Lockouts: These are remote signals which may be optionally wired to digital ground or to +5V interfaces as required to prevent local (front-panel) programming, or to prevent remote (rear-panel) programming of selected groups of functions as follows:

(1) REM PROG. SEL.: A high level disables front panel controls except POWER and RATE switches, and except those that are specifically locked out of remote operation by the following:

(2) GX: High level disables remote programming of measurand function selection;

Figure 3-1

STANDARD OUTPUT CABLE CONNECTIONS P1*

A	A (Bottom)	B	B (Top)
1	GRA	1	RANGE 10
2	INTEGRATE UNKNOWN	2	RANGE 1
3	40	3	RANGE 10K
4	800	4	RANGE 1K
5	400	5	RANGE 100
6		6	GMT
7	DIG GND INTERFACE	7	DIG GND INTERFACE
8	+5V INTERFACE	8	+5V INTERFACE
9	100	9	
10	2000	10	$\overline{\text{ARM}}$
11	80000	11	TRIGGER
12	20000	12	PROGRAM BUSY
13	OVERLOAD	13	RP BUS 6
14	+(PLUS) POLARITY	14	RP BUS 5
15	100000	15	
16	RANGE .1	16	
17	10000	17	RP BUS 4
18	40000	18	RP BUS 3
19	1000	19	RP BUS 2
20	4000	20	RP BUS 1
21	8000	21	STROBE RANGE
22	200	22	STROBE MT
23	10	23	STROBE REF
24	20	24	STROBE X
25	1	25	REM PROG SEL
26	80	26	CONVERT
27	2	27	(NOT CONNECTED)
28	8	28	
29	4	29	
30	GX	30	
31	GRC	31	
32	(NOT CONNECTED)	32	
33		33	
34		34	
35		35	
36		36	
37		37	
38		38	
39		39	
40		40	

* D.P. P/N 25-300002

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Table 3-1

REMOTE PROGRAMMING BUS FUNCTION CODING

	BUS LINES 6	5	4	3	2	1	HEX CODE
RANGE STROBE							08
R1 (10K)	1	0	0	0	0	0	40
R2 (1000)	0	1	0	0	0	0	20
R3 100	0	0	1	0	0	0	10
R4 10	0	0	0	1	0	0	08
R5 1	0	0	0	0	1	0	04
R6 .1	0	0	0	0	0	1	02
R7 AUTO RANGE	0	0	0	0	0	0	00
STROBE X							02
FØ DC	X	X	X	0	0	1	X2
F1 K	X	X	X	0	0	0	X0
F2 AC	X	X	X	X	1	X	X4
F3 TEST	X	X	X	1	0	0	X8
STROBE REF							04
F4 EXT DC	X	X	X	1	0	0	X8
F5 EXT K	X	X	X	0	0	0	X0
F6 EXT AC	X	X	X	X	1	X	X4
F7 INT REF	X	X	X	0	0	1	X2
STROBE MT							
F8 FILT IN	X	X	X	1	MT	MT	08 or MT
F9 FILT OUT	X	X	X	0	MT	MT	00 or MT
CØ 64 ms	X	X	X	F	1	0	04 or F
C1 8 ms	X	X	X	F	0	1	02 or F
C2 1 ms	X	X	X	F	0	0	00 or F

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enables front-panel control only. Low level enables either local or remote selection according to front panel selection and REM PROG SEL.

(3) GMT: High level disables remote program control of measurand integration time and of filter selection; enables either local or remote selection according to front panel selection and REM PROG SEL.

(4) GRC: High level disables remote program control of reference channel selection; enables front panel control only. Low enables either.

(5) GRA: High level disables remote program control of range; enables front panel control only. Low level enables either local or remote selection according to front panel selection and REM PROG SEL.

3.2.3 Digital Outputs.

a. General. All outputs are CMOS/DTL/TTL - compatible; ("1" $>\neq$ 2.4V, "0" $<\neq$ 0.4V); fanout 2 loads; Logic zero can sink 3.2 mA.

b. Measurement Data. Five full BCD 8-4-2-1 coded digits, sixth digit 1 bit; polarity 1 bit (high = plus).

c. $\overline{\text{OVLD}}$: 1 bit; low equals overload condition.

d. Range: 6 lines; high level indicates range in use (Ranges from .1 to 10K): Others are at low level.

e. CONVERT: High during conversion. High-to-low transition indicates end of conversion. In auto range, this line remains high until a conversion is completed on the appropriate range.

f. INTEG UNKNOWN: A flag which indicates the measurand is being integrated in phase 2 of the 4-step conversion cycle. After high-to-low transition of this line, the measurand input may be removed from the input terminals without affecting the measurement - unless auto range has been selected and the measurand is out-of-range.

g. $\overline{\text{PROG. BUSY}}$: A flag which indicates that changes of function are in progress when in low level. Multiple changes may be made while this flag is at low level. A delay of 40 milliseconds following the last change is built in to allow for completion of all changes before a measurement cycle may be initiated. Triggering is inhibited while $\overline{\text{PROG. BUSY}}$ is low.

3.2.4 Timing Waveform Diagram.

Figure 3-2 illustrates the timing relationships to be maintained for trigger control and for function programming control when in remote operation.

3.2.5 Operating Features with Basic Remote Programming Controls.

a. Making Measurements of Square Wave Amplitudes.

The Model 7500 DMM may be system-connected to perform measurements of dcv amplitudes of square waves in certain circumstances by proper selection and programming of $\overline{\text{ARM}}$, TRIGGER, and MEASUREMENT TIME.

For example, to measure the amplitude of a square-topped pulse of X msec duration, simply apply programming control signals to the rear panel connector as shown in figure 3-3. The range selected should assure an in-range measurement with the maximum possible resolution. The table in figure 3-3 relates the programmed measurement time to the duration of the signal to be measured.

Front panel trigger rate adjustment should be set at extreme counter clockwise detent for EXT RATE control.

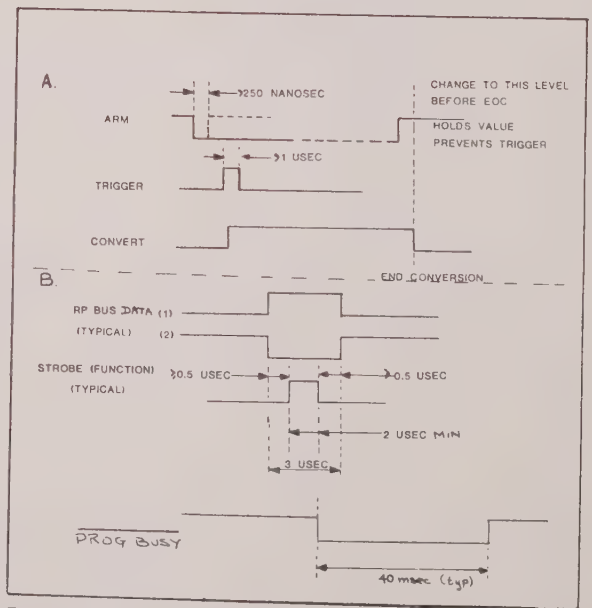

Figure 3-2. Timing waveforms for remote triggering (A) and RP Bus data transfer (B)

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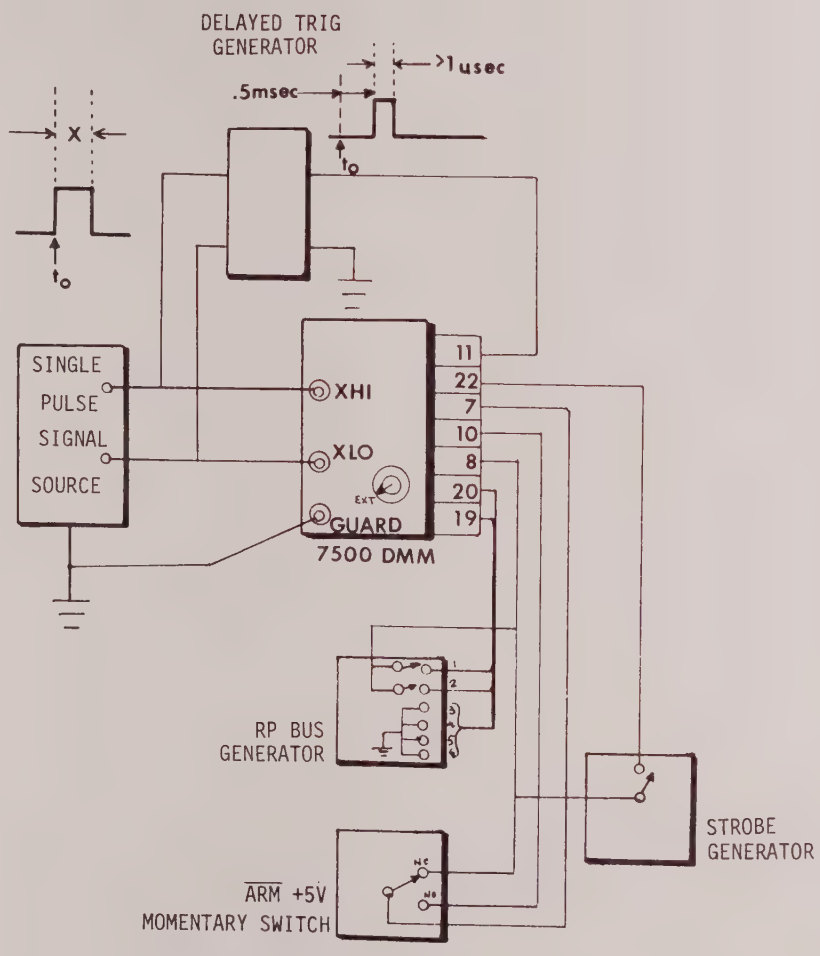

If Duration, X is between	and	Then Measurement Times should be	and RP Bus RP1	RP2
1.5 msec	8.5 ms	1 ms	0	0
8.5 msec	64.5 ms	8 ms	1	0
64.5 ms	64+ ms	64 ms	0	1

Figure 3-3. Typical connections for measuring peak amplitudes of pulse inputs.

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3.3 IEEE-488 INTERFACE, (Option D10)

3.3.1 General.

a. The two modules A10 and A11 installed in Model 7500 when Interface Option 10 is specified, provide the user with a "plug-compatible" interface with the General Purpose Interface Bus (GPIB) as defined in IEEE STD-488, standard Digital Interface for Programmable Instrumentation, dated 1975. Included in the interface installation is the installation of a receptacle mounted in rear-panel cutout. Both connector and receptacle meet requirements of Section 4 of the IEEE Standard-488. The rear panel connector terminals are internally connected to appropriate terminals of A10 by a ribbon cable.

b. Power for the interface modules is supplied from the Model 7500 power supply of + 5V supply at the rear connector. No external supply is required.

c. Simultaneous use of the IEEE-488 interface and the basic rear panel connector (para. 3.2) is limited to one unit load on the DMM 7500 data and status outputs. The Basic rear panel inputs may only be used when LOCAL is selected, with the exception of TRIGGER and ARM, which may be used in accordance with the programmed TRIGGER configuration message.

3.3.2 Terminal Connections.

a. To use the IEEE-488 interface, connect a standard IEEE-488 cable which provides signal connections as indicated in the table of Figure 3.3-1, below. Standard IEEE-488 cables in 6-ft. lengths are available as options.

Contact	Signal Line	Contact	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd. (6)
7	NRFD	19	Gnd. (7)
8	NDAC	20	Gnd. (8)
9	IFC	21	Gnd. (9)
10	SRQ	22	Gnd. (10)
11	ATN	23	Gnd. (11)
12	SHIELD	24	Gnd. LOGIC

NOTE: Gnd. (*n*) refers to the signal ground return of the referenced contact.

Figure 3.3-1. IEEE Connector terminations.

b. The address for the DMM 7500 for talk or listen is instrumented on the Module A10, by jumpers.

3.3.3 Interface Function Subsets and Messages.

a. The interface function subsets from among those available in the IEEE-488 Std that have been instrumented in the DMM 7500 are listed in Table 3.3-1. They are identified as specified in the standard.

Table 3.3.1

Ident.	Description
T5	Basic Talker including TALK ONLY and UNADDRESS IF MY LISTEN ADDRESS.
SH1	Source Handshake
L4	Basic Listener with UNADDRESS IF MY TALK ADDRESS.
AH1	Acceptor Handshake
SR1	Service Request (serial poll, full capability)
PP2	Parallel Poll (partial capability)
RL1	Remote/Local including LOCKOUT
DC1	Device Clear (selects DC INTERNAL REFERENCE, 64ms, ARMED; enables TRIGGER; clears Output Buffer).
DT1	Device Trigger
C0	No Controller Capability

b. The formats for the device dependent messages to be transmitted to the DMM 7500 from the GPIB are free-form strings. As defined in Table 3.3-2, each string consists of a function-defining alpha prefix followed by one or more coded decimal digits, if required, defining the value to be assigned to that function. Table 3.3-3 defines the Output format.

c. GPIB Programming Example.

(1) system POWER ON
7500 selects INT REF, 64 MS, DC, CLEARS last valid output buffer, places TRIGGER and ARM in high impedance states

(2) controller sends REN, IFC (holds REN for remaining steps)

(3) controller sends ATN, 7500 LISTEN address.

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Table 3.3-2
OPTION D10
Device Dependent Messages (Received by Model 7500)

Note: Ø is numeric zero; All letters are ASCII capitals; All numerals are ASCII

PREFIX LETTER	QUALIF. DIGIT	MEANING
R		RANGE PREFIX
	1	10K Range
	2	1K Range
	3	100 Range
	4	10 Range
	5	1 Range
	6	.1 Range
	7	Auto Range
F		MEASURING FUNCTION
	Ø	DC Volts
	1	Kohms
	2	AC Volts
	3	TEST
	4	EXT DC REF
	5	EXT KOHMS REF
	6	EXT AC REF
	7	INTERNAL REF
	8	Filter out
	9	Filter in
C		MEASUREMENT TIME
	Ø	64 msec
	1	8 msec
	2	1 msec
T		TRIGGER
	Ø	Normal Trigger (TRIG & ARM not driven, tristate)
	1	Immediate internal (TRIG=1, $\overline{\text{ARM}}$=0)
	2	Next external (Pulse $\overline{\text{ARM}}$, TRIG tristate)
	3	None ($\overline{\text{ARM}}$=1, TRIG tristate; Repeat last, valid out)
	4	Arm ($\overline{\text{ARM}}$=0, TRIG=tristate)
	5	Trigger on group execute trigger (Pulse $\overline{\text{ARM}}$, Pulse TRIG on GET)
M		MODE
	Ø	Address Multi. No Output
	1	Address Multi. Output
	2	Address Single. No Output
	3	Addressed Single Output
	4	Interrupt Multi. No Output
	5	Interrupt Multi. Output
	6	Interrupt Single. No Output
	7	Interrupt Single Output
E		EXECUTE

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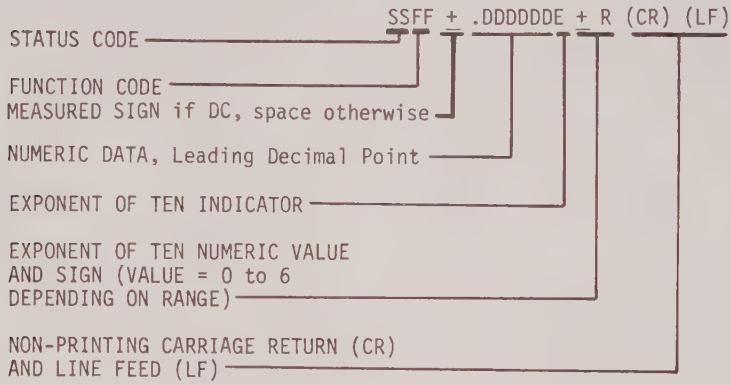
Table 3.3-3

Option D10 Output Message Formats


SSFF + .DDDDDDE + R (CR) (LF)
STATUS CODE
FUNCTION CODE
MEASURED SIGN if DC, space otherwise
NUMERIC DATA, Leading Decimal Point
EXPONENT OF TEN INDICATOR
EXPONENT OF TEN NUMERIC VALUE
AND SIGN (VALUE = 0 to 6
DEPENDING ON RANGE)
NON-PRINTING CARRIAGE RETURN (CR)
AND LINE FEED (LF)

STATUS CODE SS	DEFINITION
N (SPACE)	Normal operation; Internal reference
OL	Overload
DC	DC Reference
AC	AC Reference
KO	Kilohms Reference
E (SPACE)	Error (Commands can not be executed)

FUNCTION CODE FF	DEFINITION
AC	AC Measurand Conditioning
DC	DC Measurand Conditioning
KO	Kilohm Measurand Conditioning
T (SPACE)	Test Signal Measurand Conditioning

All Characters are transmitted in ISO-7 Bit ASCII code.

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(4) controller removes ATN, 7500 enters LISTEN ACTIVE state

(5) controller sends R5F9, T1M3, E(CR)(LF). 7500 selects 1V RANGE, FILTER IN, drives $\overline{ARM}$ and TRIGGER to 0 (trigger execution will wait til talk addressed), microprocessor selects ADDRESSED SINGLE WITH OUTPUT mode (commas, carriage return and line feed characters are ignored)

(6) controller sends ATN, UNL, voltage source LISTEN ADDRESS, 7500 stops listening while voltage source is programmed

(7) controller programs source to provide an input to 7500

(8) controller sends ATN, UNL, PRINTER LISTEN ADDRESS, controller LISTEN ADDRESS, 7500 TALK ADDRESS, 7500 enters TALK ADDRESSED state, drives $\overline{ARM}$ to 0 and TRIGGER to 1, resets $\overline{ARM}$ to 1 (single conversion mode is programmed), and waits for END OF CONVERSION and ATN to go away.

(9) controller removes ATN, 7500 enters TALK ACTIVE state, waits for END OF CONVERSION

(10) 7500 conversion ends, 7500 places status, data and function in last valid output buffer (assume +1.73506V result)

(11) 7500 sends N DC +.173506E+1 (CARRIAGE RETURN)(LINE FEED)

(12) Printer prints N DC +.173506E+1

(13) 7500 sets EOI to indicate end of message to controller

(14) controller sends ATN, UNT, 7500 EXITS TALK, waits for further commands

3.3.4 Operation Under IEEE-488 Control

Model 7500 operation in response to the decoded received messages sets up the appropriate register for Range, Measurand Selection, Reference Selection, Measure Time Selection and Filter Selection. Trigger and Mode operation are translated as described below.

3.3.4.1 Trigger Operation.

a. Trigger TØ (Regular Triggering): Conversion will proceed at the rate determined by the setting of the front-panel knob (if in Internal position). If the front-panel knob is in EXT, then the regular external TRIGGER and $\overline{ARM}$ inputs may be used to set the conversion rates, since the bus drive to those lines is in a high impedance state.

b. Trigger T1 (Immediate Internal): The bus drives TRIGGER to "1" and $\overline{ARM}$ to "0". Conversions will proceed at maximum rate consistent with measurement time in EXT; same as for TØ when front panel trigger rate control is not in EXT.

c. Trigger T2 (Next External): The bus drives $\overline{ARM}$ to "0", but TRIGGER is in high impedance state. One conversion will occur on receipt of each external trigger (or internal if not in EXT) after Execute.

d. Trigger T3 (None): The bus drives $\overline{ARM}$ to "1". The arming circuit will prevent a new conversion; data output will repeat the last valid conversion.

e. Trigger T4 (Arm): Sets up Model 7500 to perform a conversion whenever a valid TRIGGER input is received. Similar to TØ, except $\overline{ARM}$ is driven to "0" by the bus instead of passively.

f. Trigger T5 (Enable GET): Sets up Model 7500 to perform a single conversion upon receipt of Group Execute Trigger (GET) message.

3.3.4.2 Mode Operation.

a. Mode MØ (Address Multiple; No Output): Conversions are made in accordance with the trigger commands but no output data are transmitted, nor is service requested of the bus. The last valid output buffer is updated by each conversion

b. Mode M1 (Addressed Multiple: With Output): Conversions are made in accordance with the trigger commands, and data are placed on the output lines when addressed to "talk". Successive conversions are performed in accordance with the trigger commands programmed at that time up to the maximum rate at which the bus will accept data. If Trigger Mode is T1 or T4, the conversion trigger will be disarmed until the data is accepted by the bus when necessary. In other Trigger Modes, data from those conversions which exceed the bus capacity will be ignored.

c. Mode M2 (Addressed Single with No Output): A single conversion is made in the programmed Trigger Mode. The data of the

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measurand value is placed in the last valid output buffer, but is not put on the bus, nor is service requested.

d. Mode M3 (Addressed Single with Output): Model 7500 makes a conversion when addressed to "talk" and triggered and places the measurand data values on the output lines. Each successive conversion requires a programmed command of EXECUTE when in this mode. if it is to be output to the bus.

e. Model M4 (Interrupt Multiple with No Output): Operation is same as for Mode MØ.

f. Mode M5 (Interrupt Multiple with Output): Operation is same as for Mode M1, except that Model 7500 will send a service request command (SRQ low) if not addressed to talk at the end of each conversion. The SRQ line will be changed to a high level after the data values have been outputted by the Model 7500 or after a serial poll of the unit.

g. Mode M6 (Interrupt Single with No Output): Operation is same as that in Mode M2.

h. Mode M7 (Interrupt Single with Output): Operation is same as that in Mode M3, except that Model 7500 will send a service request command (SRQ low) if not addressed to talk when the conversion is completed. (See

3.3.5 REMOTE-LOCAL BUS CONTROL

The D10 option provides a complete RL1 interface function capability. Four interface states exist: local, remote, local with lockout, and remote with lockout. The front panel local switch and associated indicator do not directly indicate which interface state is active since the Model 7500 can also operate remotely using its standard parallel interface while an inactive D10 interface is present.

Local State - When the interface is not receiving REN from the bus or when power is first applied the interface is in the local state. In the local state operating the local pushbutton alternately switches the Model 7500 between local (front panel) control and parallel interface (rear connector) control. If the bus sends REN and the 7500 listen address the interface pulses remote program select and enters the interface remote state. Pulsing remote program select causes the 7500 local indicator to go out if it was on initially. If the bus sends REN and then LLO (ASCII device control character DC1) the interface enters the local with lockout state. The 7500 local indicator does not change, remaining either on or off. If the talk only switch is on, no messages are output while local is selected from the front panel.

Remote State - In this state the interface controls all the programmable functions of the 7500, and the local indicator is off. No functions other than local are changed on entry. Control settings are held until changed by commands from the bus. Pushing the local switch returns the 7500 and the interface to local state, turning on the local indicator. Sending GTL (ASCII character, SOH) returns the interface to the local state but does not turn on the 7500 local indicator until the local switch is pushed. Sending LLO causes the interface to enter remote with lockout. If the talk only switch is on, measurement data are transmitted to the bus while in remote.

Remote with Lockout State - In this state the interface controls all programmable functions of the 7500 and the local indicator is off. In this state the interface continually sends remote prog. select which disables the front panel local switch. If the bus sends GTL it causes the interface to enter the local with lockout state.

Local with Lockout State - In this state the local pushbutton switches the 7500 between local (front panel) and remote (rear parallel interface connector) control. When this state is entered from remote lockout the local indicator is initially off, while entry from local leaves the local indicator in whichever condition was present. If the bus sends the 7500 listen address the interface enters the remote with lockout state.

3.3.6 PARALLEL POLL

The D10 interface provides the PP2 and partial PP1 capabilities when a selection jumper is installed. As shipped with no jumper the configuration is PPØ. The only exception to full PP1 capability is that the PPR message selection must be performed by a jumper wire instead of configuring by the 3 low order bits of the PPE command. The sense bit of the PPE command does configure the parallel poll response. Therefore the parallel poll active state sends the jumper selected PPR message true if the sense bit is one and the 7500 is requesting service or if sense is zero and the 7500 is not requesting service. Otherwise the message is passive false. The interface CPU responds to all parallel poll related commands including PPE, PPD, PPU, PPC at all times but can not transmit any response message until the message selection jumper is installed.

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3.3.7 SERVICE REQUESTS

The D10 interface can request service in two ways, via the SRQ uniline message and, when properly configured and polled via the parallel poll discussed above. Service requests are initiated by the D10 interface under two circumstances: (1) when an interrupt mode has been programmed, a new data word is available and the Model 7500 is not addressed to talk; and (2) when an error in programming is detected, the Model 7500 is not addressed to talk, and the EREN jumper, A10-W1 is in its normal position between A10-E16 and A10-E17. If A10-W1 is cut and A10-E16 jumpered to A10-E18 these error service requests are suppressed.

A service request initiated by the Model 7500 is reset by a serial poll of the 7500, a parallel poll, being addressed to talk, entering the addressed to listen state, device clear, or selective device clear. If the service request is due to a programming error the status word sent in response to a serial poll will have BIT 8 set as well as RQS, BIT 7. If the request is due to new data availability in interrupt mode only RQS, BIT 7, will be set.

3.3.8 FIELD INSTALLATION

Refer to Assembly Dwg. D57-1088 for locations and parts list PL50-1088 for identification of the parts provided. Before installing the interface I/O section, A10, install the configuration control jumpers for the following functions: AD1 through AD5 for device address selection, W8 for parallel poll response message. Coding for these jumpers is listed in Table I and Table II. Before installing the microprocessor section, A11, install the configuration control jumpers for the 7500 signal conditioning options installed. Coding for these jumpers is listed in Table III.

If it is desired to suppress service requests on programing errors cut etch jumper W1 between E16 and E17 on A10 and install a wire jumper from E16 to E18 instead.

Remove the blank connector cover plate from the rear panel of the 7500 and install the replacement plate bearing the output connector, cable, and talk only switch (Assy D57-1095). Plug the other end into A10J1. Observe polarity of connector. Connect power cable A11 P3 to power supply A15P6. If necessary solder A15P6 cable assy to power supply terminals E23 and E27 shown in view A-A on installation assembly drawing D57-1088. Install interconnect ribbon jumper cable WL between A10J2 and A11J2. Check that A10 and A11 are firmly seated in their correct locations.

```
* * * * * * * * * * * * * * * * * * * * * * * *
*                                               *
*                  C A U T I O N                *
*                                               *
*  To avoid permanent damage to the MOS         *
*  integrated circuits be sure that any         *
*  soldering iron used on these cards has       *
*  a grounded tip.  Short all PC connector      *
*  tabs with conductive foil while solder-      *
*  ing.  Do not remove or install PC cards      *
*  or internal connection cables with pow-      *
*  er on.                                       *
*                                               *
*                                               *
* * * * * * * * * * * * * * * * * * * * * * * *
```


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Table 3.3-4

JUMPERS FOR FUNCTIONS AD1 THROUGH AD5

TALK ADDRESS ASCII CHARACTER	LISTEN ADDRESS ASCII CHARACTER	AD1 CONNECT E11 to	AD2 CONNECT E12 to	AD3 CONNECT E14 to	AD4 CONNECT E15 to	AD5 CONNECT E13 to
@	SP	E31	E32	E34	E35	E33
A	!	E21	E32	E34	E35	E33
B	"	E31	E22	E34	E35	E33
C	#	E21	E22	E34	E35	E33
D	$	E31	E32	E24	E35	E33
E	%	E21	E32	E24	E35	E33
F	&	E31	E22	E24	E35	E33
G	'	E21	E22	E24	E35	E33
H	(	E31	E32	E34	E25	E33
I	)	E21	E32	E34	E25	E33
J	*	E31	E22	E34	E25	E33
K	+	E21	E22	E34	E25	E33
L	,	E31	E32	E24	E25	E33
M	-	E21	E32	E24	E25	E33
N	.	E31	E22	E24	E25	E33
O	/	E21	E22	E24	E25	E33
P	0	E31	E32	E34	E35	E23
Q	1	E21	E32	E34	E35	E23
R	2	E31	E22	E34	E35	E23
S	3	E21	E22	E34	E35	E23
T	4	E31	E32	E24	E35	E23
U	5	E21	E32	E24	E35	E23
V	6	E31	E22	E24	E35	E23
W	7	E21	E22	E24	E35	E23
X	8	E31	E32	E34	E25	E23
Y	9	E21	E32	E34	E25	E23
Z	:	E31	E22	E34	E25	E23
[	;	E21	E22	E34	E25	E23
		E31	E32	E24	E25	E23
]	=	E21	E32	E24	E25	E23
		E31	E22	E24	E25	E23
DO NOT USE	DO NOT USE	E21	E22	E24	E25	E23

Table 3.3-5

PARALLEL POLL RESPONSE MESSAGE SELECTION

MESSAGE M NEMONIC	MESSAGE NAME	CONNECT JUMPER W8 FROM E1 TO
PPR1	PARALLEL POLL RESPONSE 1	E2
PPR2	PARALLEL POLL RESPONSE 2	E3
PPR3	PARALLEL POLL RESPONSE 3	E7
PPR4	PARALLEL POLL RESPONSE 4	E8
PPR5	PARALLEL POLL RESPONSE 5	E4
PPR6	PARALLEL POLL RESPONSE 6	E5
PPR7	PARALLEL POLL RESPONSE 7	E6
PPR8	PARALLEL POLL RESPONSE 8	E9
NUL	NULL BYTE (NO RESPONSE)	NO W8 CONNECTION

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Table 3.3-6

All OPTION JUMPERS

OPTION INSTALLED		JUMPER A		JUMPER B		JUMPER C	
		FROM E-	TO E-	FROM E-	TO E-	FROM E-	TO E-
	NOTE 1						
AC Ø		43	53	-	-	-	-
AC 1		43	63	-	-	-	-
AC 2		43	63	-	-	-	-
K Ø		47	57	-	-	-	-
K 1		47	67	-	-	-	-
RDC ØØ	NOTE 2	44	54	45	55	46	56
RDC Ø1		44	54	45	65	46	56
RDC Ø2		44	54	45	65	46	56
RDC Ø3		44	64	45	65	46	56
RDC Ø4		44	64	45	65	46	56
RDC Ø5		44	54	45	55	46	66
RAC ØØ		40	50	41	51	42	52
RAC Ø1		40	60	41	51	42	52
RAC Ø2		40	50	41	61	42	52
RAC Ø3		40	60	41	61	42	52
RAC Ø4		40	50	41	51	42	62
RAC Ø5		40	60	41	51	42	62
RAC Ø6		40	60	41	51	42	52
RAC Ø7		40	50	41	61	42	52
RAC Ø8		40	60	41	61	42	52
RAC Ø9		40	50	41	51	42	62
RAC 1Ø		40	60	41	51	42	62
RK ØØ	NOTE 2	44	54	45	55	46	56
RK Ø1		44	64	45	55	46	56
RK Ø2		44	54	45	65	46	56
RK Ø3		44	64	45	65	46	56
RK Ø4		44	54	45	55	46	66
RK Ø5		44	64	45	55	46	66
RK Ø6		44	54	45	65	46	66

NOTE 1: Install only the jumpers for the one option occupying a card slot at any time.

NOTE 2: Install these jumpers only if no other RDC or RK option is installed.

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DIO OPTION COMMANDS

Table 3.3-7

Standard Multiline Interface Messages
(Received by Model 7500 when transmitted with ATN=1 by the controller. Bit DIO-8 is ignored for all commands.)

HEXADECIMAL CODE (DIO1 - DIO7)	ISO/ASCII CHARACTER	MESSAGE MNEMONIC & DESCRIPTION (IEEE 488)
ADDRESSED COMMAND GROUP (Ignored if not addressed to listen.)		
01	SOH	GTL - go to LOCAL, enable front panel controls.
04	EOT	SDC - Selective Device Clear; clears service requests, last valid conversion buffer, sets $\overline{ARM}$ = 0, set TRIG drive to open-circuit state, select DC, INT REF, 64 mS, AUTORANGE, FILTER OUT
05	ENQ	PPC - Parallel Poll Configure; preparatory command required for Parallel Poll Enable or Disable to be recognized.
08	BS	GET - Group Execute Trigger
09	HT	TCT - Ignored by Model 7500 always

HEXADECIMAL CODE (DIO1 - DIO7)	ISO/ASCII CHARACTER	MESSAGE MNEMONIC & DESCRIPTION
UNIVERSAL COMMAND GROUP		
11	DC1	LLO - Local Lockout; inhibits return to LOCAL from REMOTE by front panel LOCAL switch.
14	DC4	DCL - Device Clear; same action as SDC above.
15	NAK	PPU - Parallel Poll Unconfigure; disables all parallel poll response messages.
18	CAN	SPE - Serial Poll Enable
19	EM	SPD - Serial Poll Disable
3F	?	UNL - Unlisten
5F	_	UNT - Untalk
ADDRESSED COMMAND GROUP		
20 - 3E 40 - 5E		LISTEN ADDRESSES-)One value selected TALK ADDRESSES -)by jumpers for 7500 listen address. Talk address is listen address plus 20 (Hexadecimal)
SECONDARY COMMAND GROUP (Require PPC command prefix)		
60	' (Single Open Quote)	PPE - Parallel Poll Enable with sense bit ZERO
61	a	"
62	b	"

HEXADECIMAL CODE (DIO1 - DIO7	ISO/ASCII CHARACTER	MESSAGE MNEMONIC & DESCRIPTION
63	c	PPE - Parallel Poll Enable, with sense bit ZERO
64	d	"
65	e	"
66	f	"
67	g	"
68	h	PPE - Parallel Poll Enable, with sense bit ONE
69	i	"
6A	j	"
6B	k	"
6C	l	"
6D	m	"
6E	n	"
6F	o	"
70	p	PPD - Parallel Poll Disable

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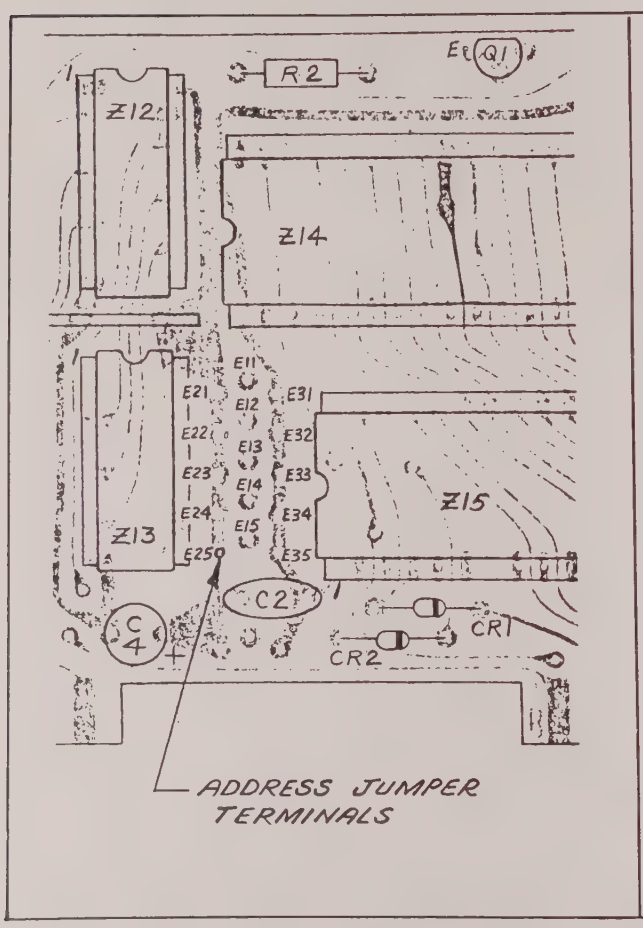
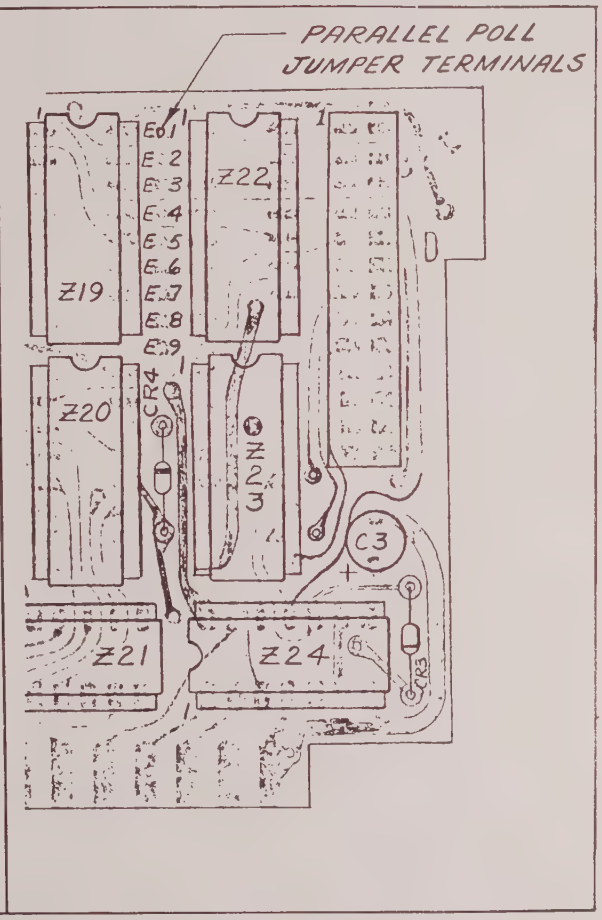


D10 Option Address Jumper Terminals



D10 Option Parallel Poll Jumper Terminals

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3.4 OPTION D30, RS232/TTY INTERFACE

3.4.1 General

a. The Model 7500/D30 combination provides its RS232C output on an ITT/Cannon type DB25-P* connector or equivalent. This provides for direct connection to a modem using RS232C assigned pin numbers on a pin-for-pin basis, with the 7500 acting as a data terminal equipment (DTE) and the modem as data communication equipment (DCE). For direct connection to a computer RS232C or other terminal interface configured as a DTE, a special cable may be required with sending and receiving directional signals interchanged. If some interface signals are missing, they may require jumpers to other signals, which are present.

b. The RS232 signal lines which are implemented in hardware in this option are listed in Table 3.4-1. Hardware implementation does not mean that the DATA PRECISION provided standard software/firmware supports the use of all lines indicated in the table, only that suitable software/firmware can detect or send signals, as tabulated. All RS232 lines not tabulated are not connected and not terminated in the Model 7500. The teletypewriter interface connector provides for a 20mA current loop driver for output to the printer and an independent 20mA current loop input from the keyboard or tape reader. Pin assignments for this Amphenol type 223-1505† connector or equivalent are listed in Table 3.4-2. The teletypewriter is assumed to always operate in full duplex mode.

c. Data source selection is jumper and firmware controlled. A jumper selects whether RS232 or the TTY is the input source to be selected at power on. Software commands received from that source can then switch between inputs. All data output is directed to both the teletypewriter and the RS232 connectors simultaneously, but RS232 control signals DATA SET READY, DATA CARRIER DETECT and CLEAR TO SEND are ignored when teletypewriter is selected and DATA TERMINAL READY is false.

Consult Data Precision if the requirements of your system conflict with this standard firmware program procedure.

d. The standard D30 option includes an MC6800 microprocessor with 2K words (8 bits per word) of socket mounted read only memory firmware and 128 words of random access memory. An additional socket is provided for user ROM memory expansion to a total of 3K words. All 3 ROM sockets are compatible with type 2708 ultraviolet eraseable, electrically reprogrammable 1K x 8 read only memories, or mask programmed equivalents.

e. The Model 7500/D30 basic hardware with different ROM firmware installed is capable of supporting the ANSI standard data communication procedures of x3.28-1976. Since many variations are possible within the scope of the standard, consult DATA PRECISION CORPORATION about particular requirements.

3.4.2 Option D30 Firmware

a. The firmware assumes a dedicated two-station configuration. Figure 3.4-1 illustrates the processing described in the paragraphs that follow.

b. In half duplex operation, upon power application the Model 7500/D30 transmits a prompting message to the selected source, assuming master station status for RS232 operation. It then relinquishes its master status and awaits a command string from the controller. A command string consists of no more than 31 characters of prefix letters and qualifier digits selected from Table III, followed by a carriage return character. Upon receiving the carriage return character the Model 7500/D30 first transmits a carriage return followed by a line feed character, then either a measurement response message sequence if one or more valid Execute (E) commands were received or an error message if necessary, and, finally, a new prompting message. The Model 7500/D30 then stops transmitting and awaits a new command string. If a D5 message is included in the command string all subsequent characters in the string other than the carriage return or an H are ignored and following the RS232 hang up sequence the program restarts as if power were turned on at that point. If an H character is included in the command string the H and all prior characters are removed from the pending command buffer immediately without waiting for a carriage return.

c. In full duplex, operation is the same as described in b. above with the following exceptions:

(1) Each received command string character is echoed when received, except H.

(2) A multiple measurement mode may be selected which results in continuous output of measurements as the Model 7500 makes them for a single E command. In multiple measurement modes, reception of an H character will cause the Model 7500/D30 to halt if transmitting. It will then wait for new commands. Note that commands subsequent to the multiple measurement will not be executed since the H also cancels them.

---

*Mating connector: ITT type DB25-S

†Mating connector: Strain relief Amphenol 223-21-1, body Amphenol 223-1605, pins Amphenol 220-830-07

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TABLE 3.4-1

Option D30 RS232 Interface Circuits

Pin No.	Circuit	Description	Direction	Notes
1	AA	Protective Ground	Not applicable	1
2	BA	Transmitted Data	From 7500 to DCE	1
3	BB	Received Data	From DCE to 7500	1
4	CA	Request to Send	From 7500 to DCE	
5	CB	Clear to Send	From DCE to 7500	1, 2
6	CC	Data Set Ready	From DCE to 7500	1, 3
7	AB	Signal Ground	Not Applicable	1
8	CF	Received Line Signal Detector	From DCE to 7500	1, 3
20	CD	Data Terminal Ready	From 7500 to DCE	
21	CG	Signal Quality Detector	From DCE to 7500	
22	CE	Ring Indicator	From DCE to 7500	

NOTES

1. Required signals for operation of D30.
2. Connect to circuit CA if not provided by DCE.
3. Connect to circuit CD if not provided by DCE.

TABLE 3.4-2

Option D30 Teletypewriter Interface Circuits

Pin	Description
1	Shield
2	TTY Printer Return -12V
3	TTY Printer Data, 7500 Output
4	TTY Keyboard Return -12V
5	TTY Keyboard Data, 7500 Input

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3.4.3 Error Conditions.

a. Communication Error conditions include reception of a character with incorrect parity, input overrun, framing error of an input character, loss of carrier on RS232 reception. Command error conditions include reception of a letter which is invalid as a command, reception of a digit without a valid prefix letter, and reception of a digit greater than allowed for the active prefix. Measurement error conditions include any attempts to measure using a signal conditioning option which is not installed.

b. Reception of a character with incorrect parity will cause the D30 processor to mask the parity bit and attempt to interpret the character based on the remaining bits. If the result is a valid command string it will be executed at the following carriage return but a question mark will be transmitted after the carriage return/line feed before any output or the next prompt. If the command string resulting is invalid, the first invalid character will be transmitted preceded and followed by question marks. Any valid commands preceding the invalid character will be executed, all other commands in the string are ignored, and a new prompt character is sent.

c. Input overrun or framing errors when detected by the D30 processor are treated just as parity errors are except that an asterisk is substituted for the unknown character and is always invalid.

d. Loss of carrier during reception or full duplex operation causes an attempt to recover after a fixed delay. If the carrier has been restored at the end of the delay an asterisk is substituted for any character lost and operation continues as in a frame error. If carrier is still lost after the delay the processor attempts to restart just as if power was being turned on initially, and all pending commands are lost. The restart returns control to the jumper selected input source. Any command error causes the first invalid character to be transmitted followed by a question mark. Any earlier valid commands are executed while the invalid character and its successors are ignored except for H. A command error followed by an H is ignored as are all command characters followed by an H. A command string too long to fit the input buffer causes a question mark to be transmitted following reception of a carriage return and prior to execution of those portions of the string which were received prior to buffer overflow.

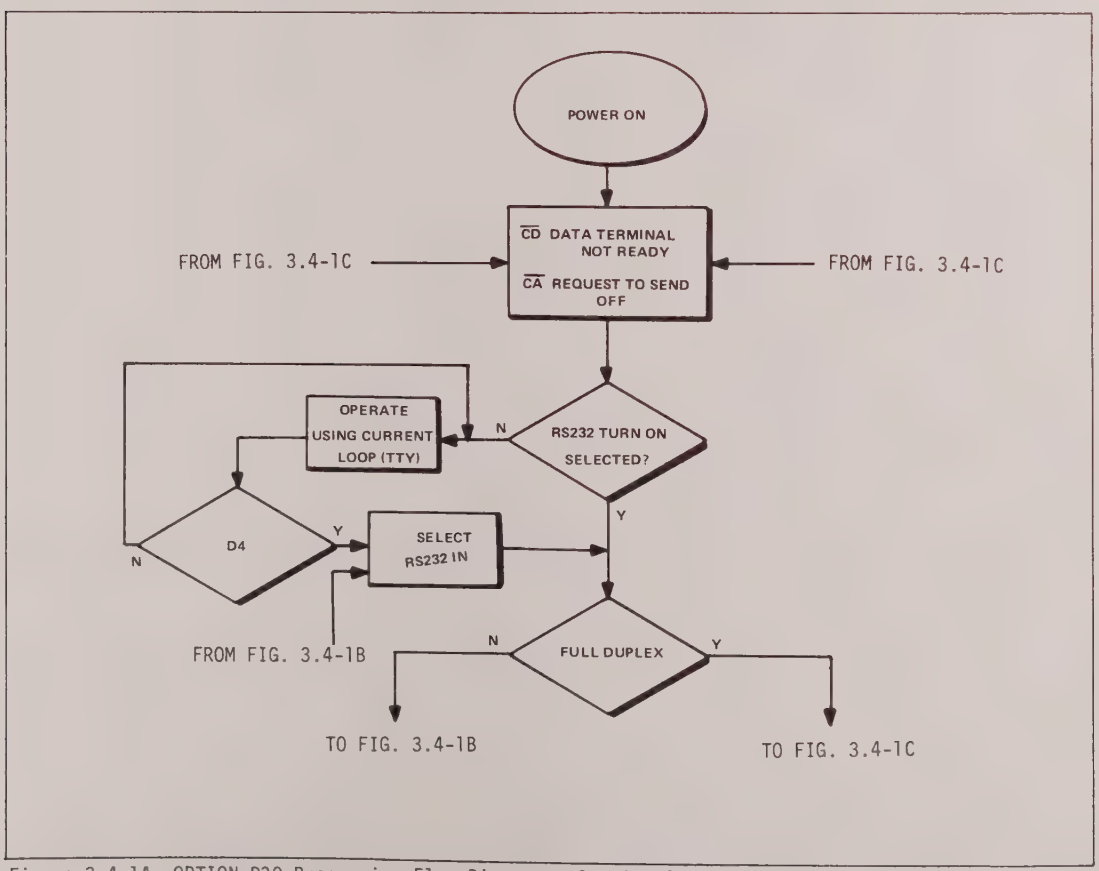

Figure 3.4-1A OPTION D30 Processing Flow Diagram - Getting Started

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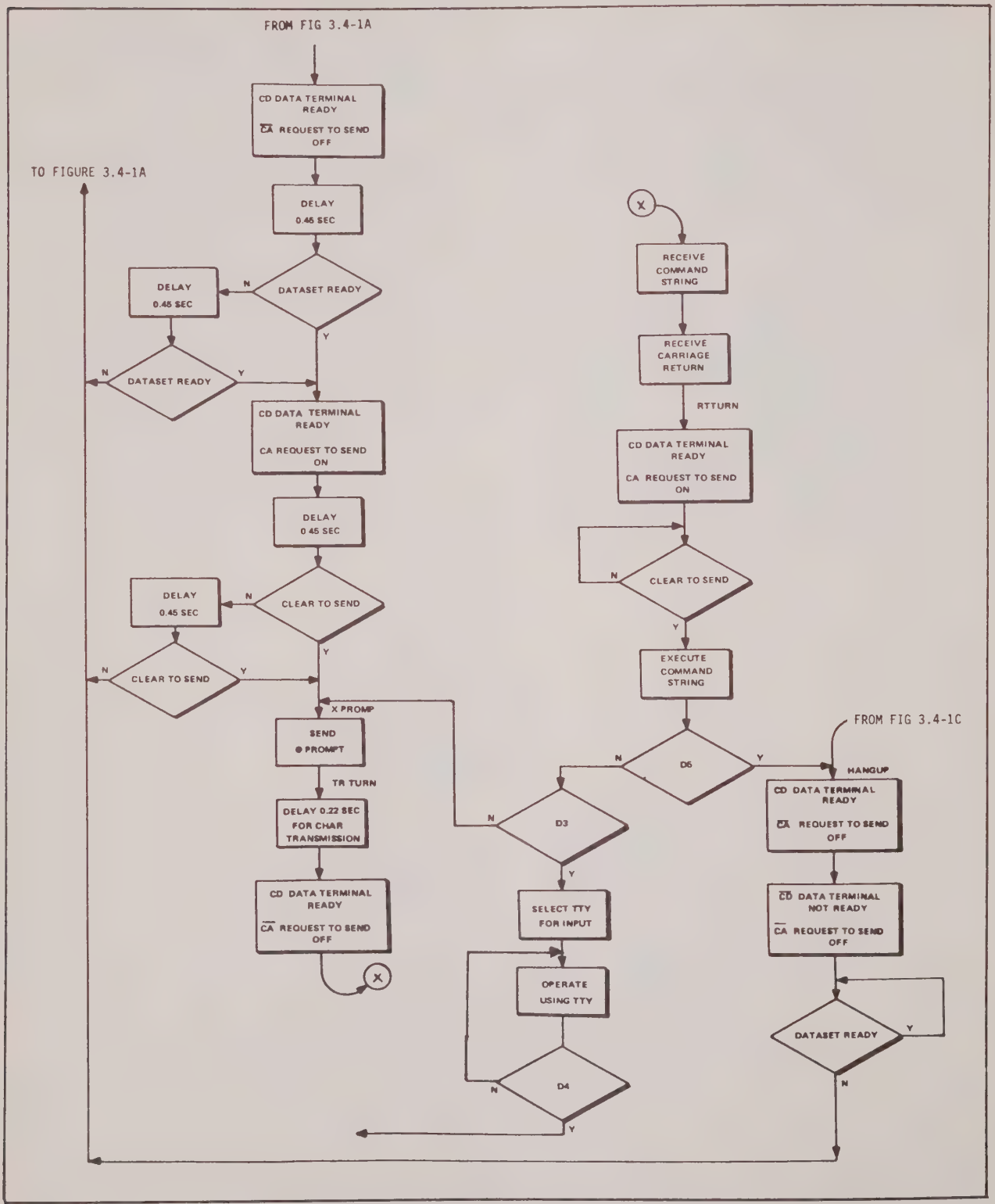

Figure 3.4-1B OPTION D30 Processing Flow Diagram - Half Duplex

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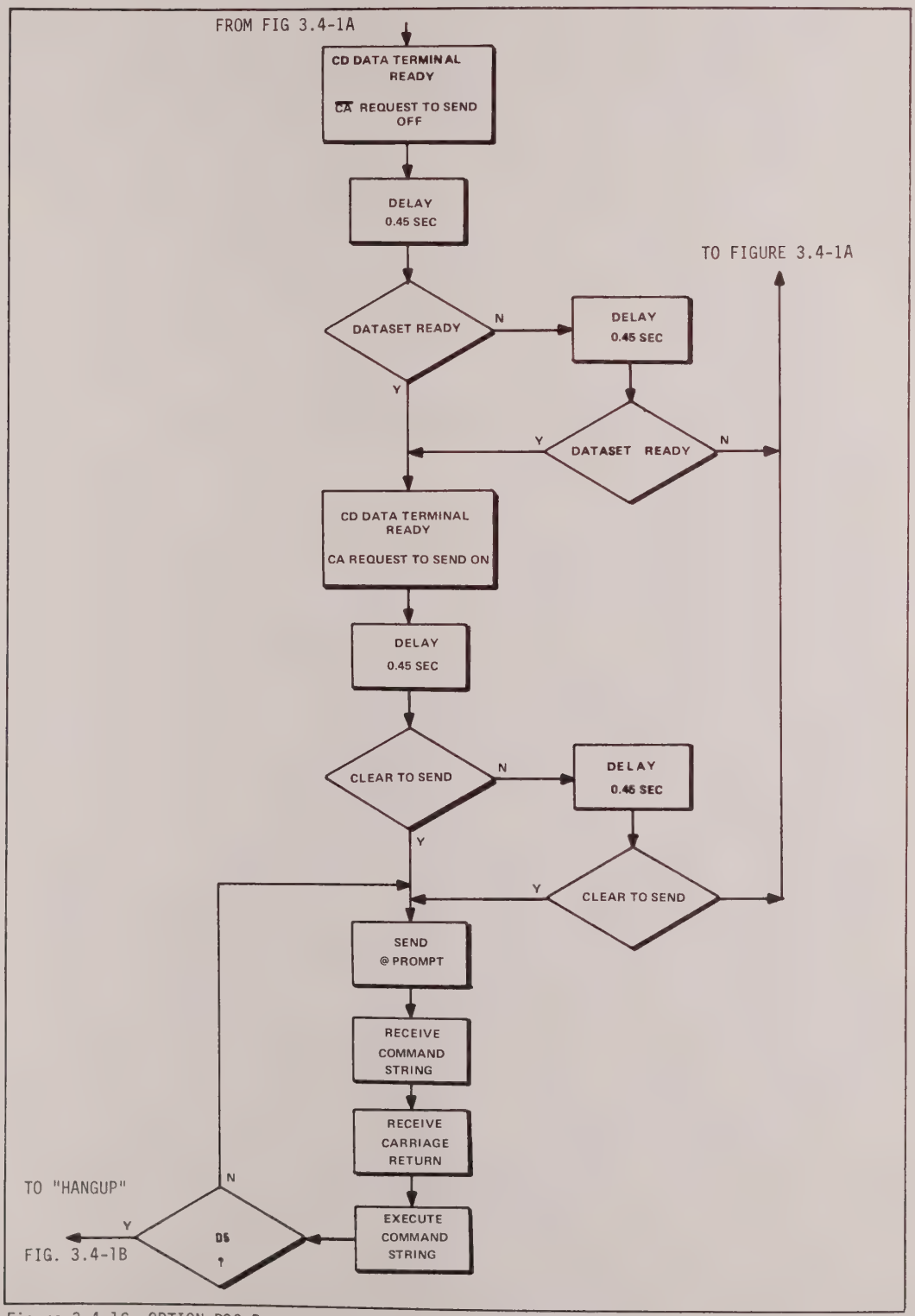

Figure 3.4-1C OPTION D30 Processing Flow Diagram - Full Duplex

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Table 3.4-7

COMMUNICATION CONFIGURATION CONTROL JUMPERS

GND TERMINAL	JUMPER A FUNCTION	FUNCTION TERMINAL	JUMPER B FUNCTION	+5 TERMINAL
E31	No Parity	E11	Parity	E21
E32	Current Loop	E12	RS232	E22
E33	Odd Parity	E13	Even Parity	E23
E34	Half Duplex	E14	Full Duplex	E24
E35	1 Stop Bit	E15	2 Stop Bits	E25
E36	8 Bit Spaces	E16	8 Bit Marks	E26

Notes:

1. Install either a jumper A or a jumper B for each function terminal but not both.

2. The E13 selection is effective only when parity is selected, while the E16 selection is effective only when no parity is selected.

3. Half/Full Duplex selection affects only RS232 operation. Current loop operation is always full duplex.

4. See Figure 3.4-2 for terminal location view.

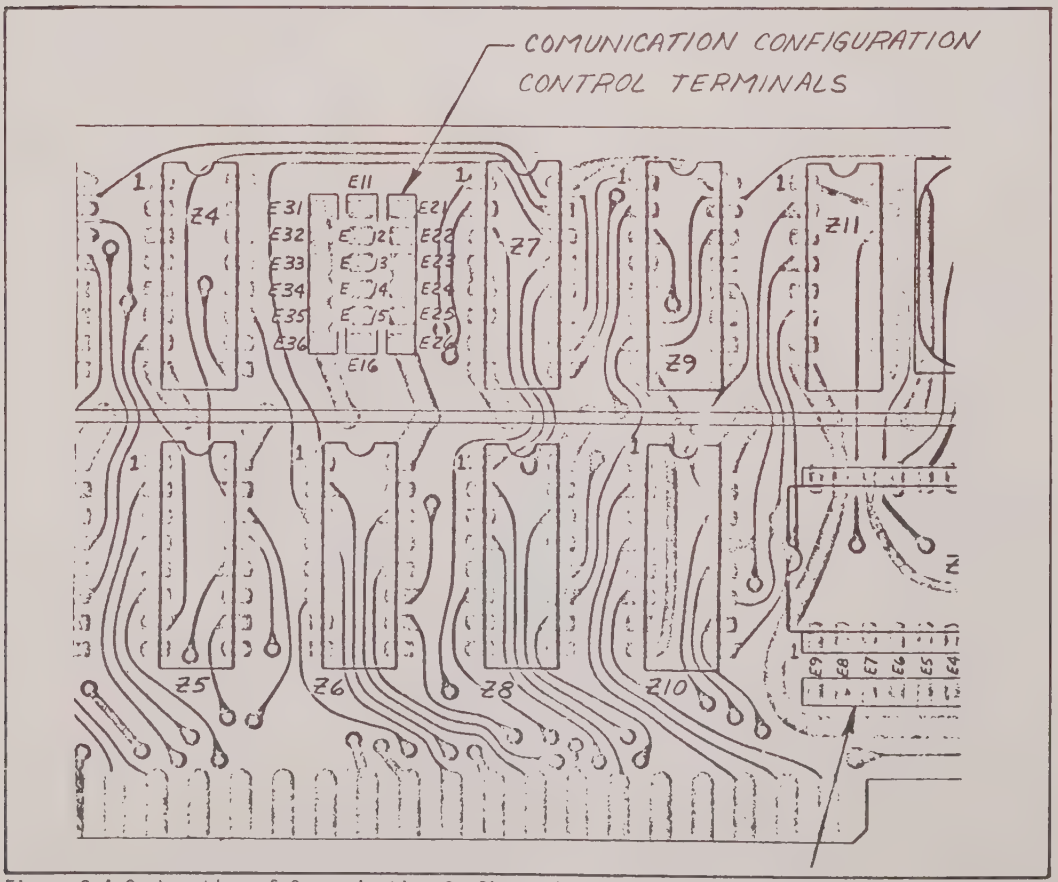

Figure 3.4-2 Location of Communication Configuration Control Terminals

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Table 3.4-8

BAUD RATE SELECTION JUMPER

Baud Rate	Connect E1 to
110	E2
150	E3
300	E4
600	E5
1200	E6
2400	E7
4800	E8
9600	E9

Notes:

1. Install only one jumper at any time.
2. See Figure 3.4-3 for terminal location view.

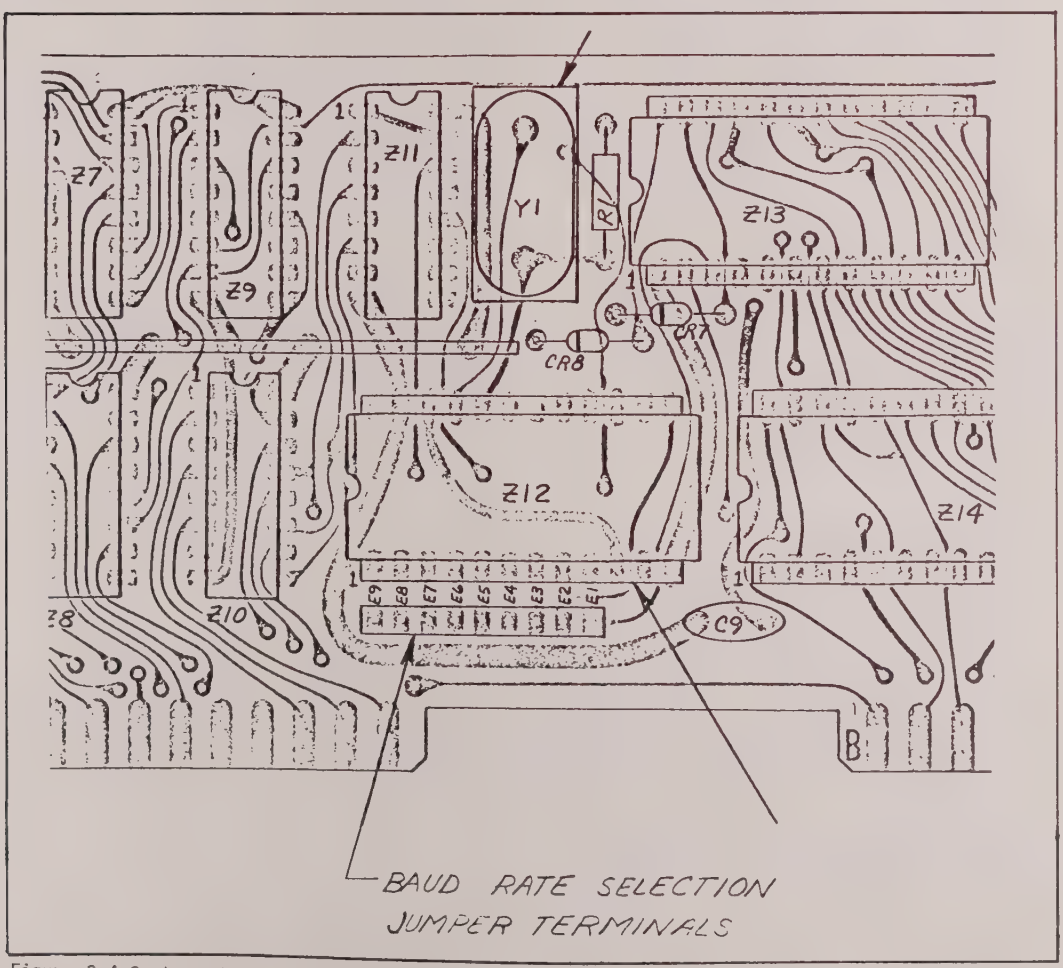

Figure 3.4-3 Location of BAUD RATE Selection Jumper Terminals

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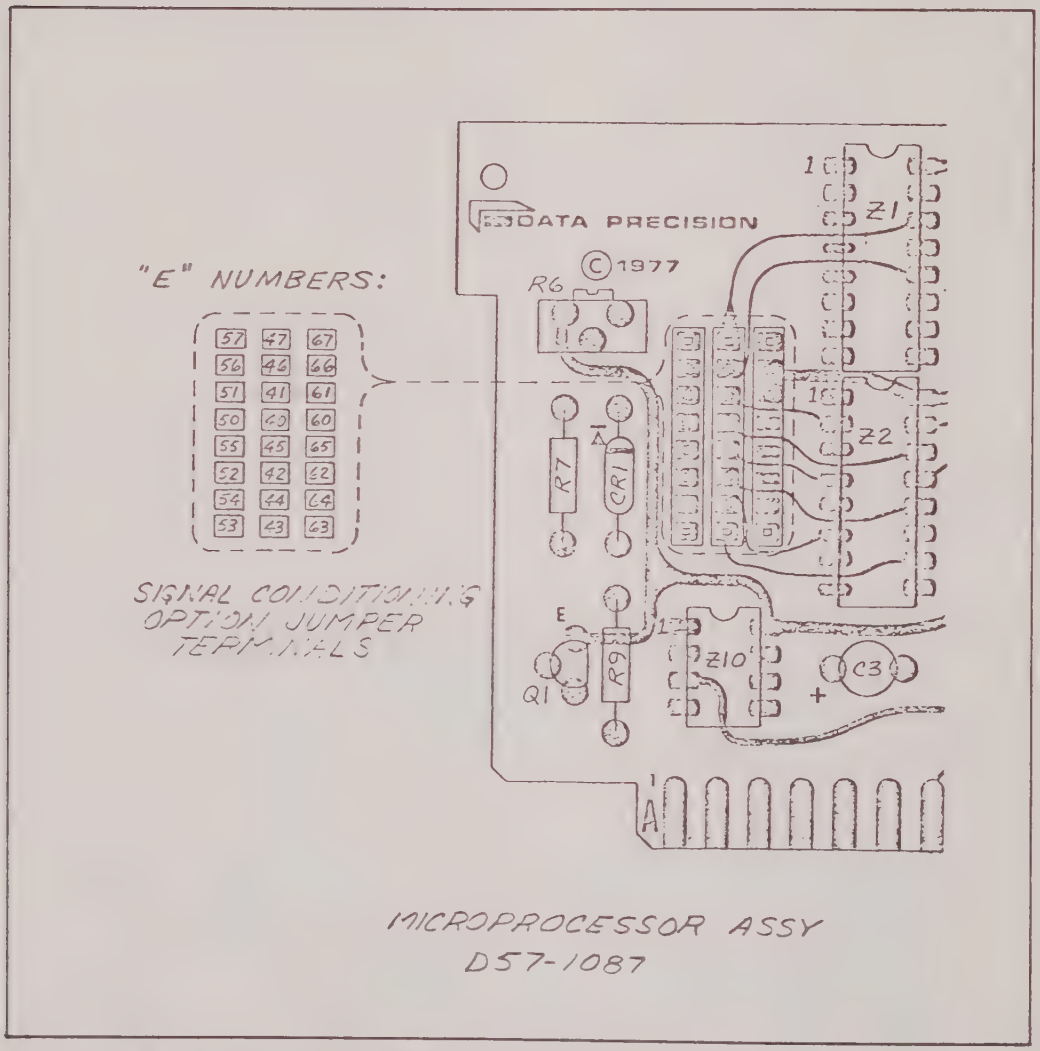

Figure 3.4-4 Location of Signal Conditioning Option Jumper Terminals in Microprocessor Assembly

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e. A measurement error is reported via an E as the first character of the format in an output measurement with status, M2, M3 or a status output, M6.

3.4.5 Sample user/7500 Dialogue for D30 Option

a. We assume an installation configured as shown in Figure 3.4-5, wherein a Model 7500 with Option D30 installed is connected to interface with an RS232-compatible terminal. We further assume that the system is set up for Full Duplex operation, and the jumpers have been installed for TTY initial selection as input source.

b. When POWER is turned ON, the Model 7500/D30 sends the character "@" to both the TTY and RS232 terminals, but is expecting initial input from the TTY and ignoring RS232 input.

c. The TTY operator starts by selecting REMOTE control of the Model 7500 by sending: (In Full Duplex, all characters, other than H, (CR), and (LF) are echoed back to the TTY as soon as received.)

D1(CR)

d. The 7500 responds by turning OFF its LOCAL light, and then sends:

(CR)(LF)@

(Note that this (CR) is the echo of that sent by the TTY.)

e. The TTY operator wants to prepare to make a series of single dc measurements using the D30 to trigger each measurement of a dc signal on the 1-volt range at the 64 msec rate with FILTER selected. He sets the EXT RATE control to EXT and sends:

M2R5CØFØ79T5(CR)

(Note this string must not exceed 31 characters but the sequence is not important except that qualifier digits must follow the correct prefix character.)

f. The 7500 goes to the 1-volt range, DC, INTERNAL REFERENCE, FILTERED. The D30 processor sets up for data rate retrigger and single measurements with status output, then responds with:

(CR)(LF)@

g. The TTY operator sends:

EEE(CR)

h. The 7500 responds by making 3 measurements (assume a 1-volt signal) sending:

(CR)(LF)NDC +.100000E +1(CR)(LF)
NDC +.100000E +1(CR)(LF)
NDC +.100000E +1(CR)(LF)
@

(Note with T5 the second measurement is triggered after transmission is started of the (CR) of the first measurement. Since the (LF) character is buffered on output by the ACIA of the D30 circuit.)

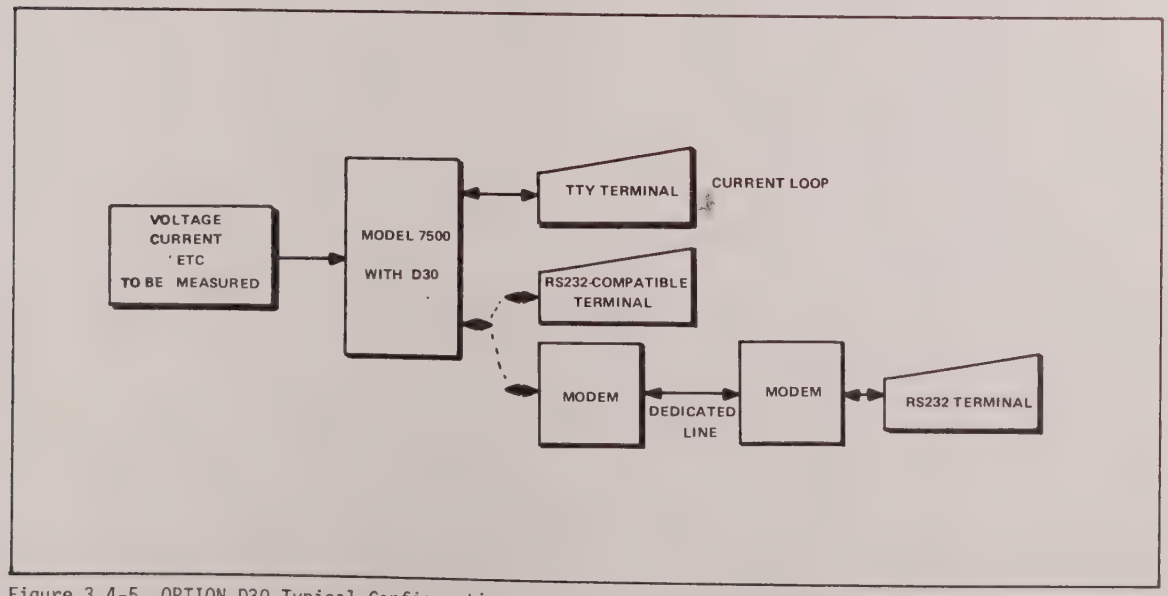

Figure 3.4-5 OPTION D30 Typical Configuration

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i. To transfer control to the RS232 Terminal, the TTY operator types:

D4(CR)

j. The 7500 selects the RS232 Terminal for input and sends:

(CR)(LF)@

(Note this still prints on the TTY, but the TTY Keyboard is dead.)

k. If the RS232 Terminal controller wants to measure the ac ripple on the input voltage, it sends:

R6F2E(CR)

l. The 7500 goes to AC (Filter is always OUT on AC), 0.1V RANGE, and makes a measurement using the previously programmed CONVERT TIME, TRIGGER Mode, and MEASUREMENT Mode, then sends:

(CR)(LF)N AC .000250E +0(CR)(LF)

@

(Note, this still prints on the TTY)

m. To return control to the TTY operator the RS232 source sends:

D3(CR)

n. The 7500 selects the TTY for input and sends:

(CR)(LF)@

o. The TTY operator sends:

QR7T3M6HR7T3M3(CR)

p. The 7500 ignores (but has echoed) QR7T3M6, the executes R7T3M3 by selecting AUTORANGE, Disarming TRIGGERS, and preparing for multiple measurements, then sends:

(CR)(LF)@

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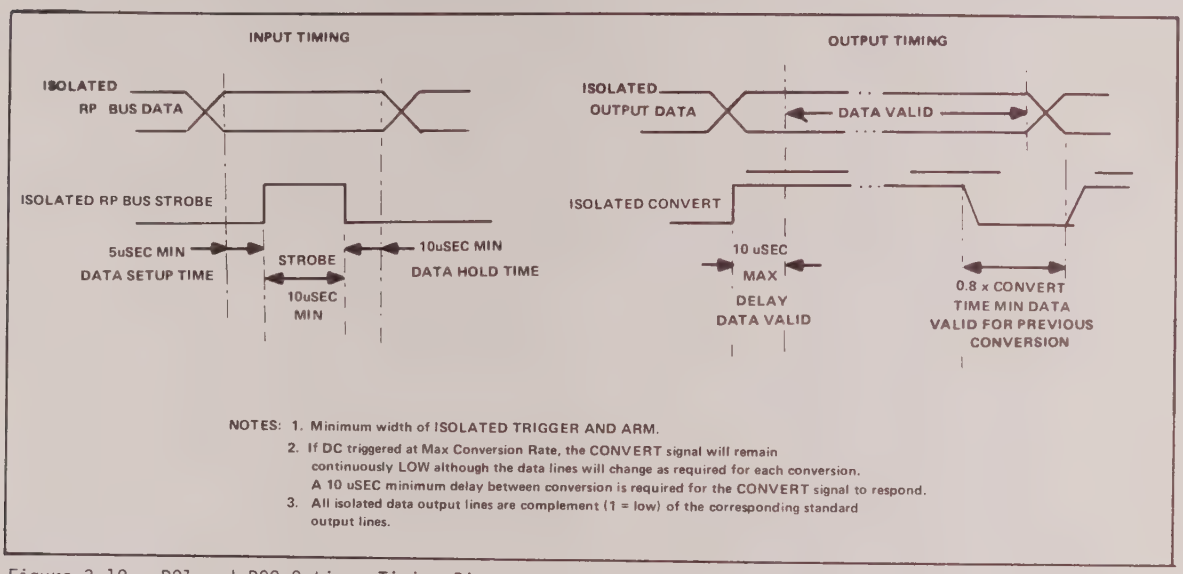

Figure 3.10 D01 and D02 Options Timing Diagram

I10 CONNECTIONS FOR D01, D02 OPTIONS

A15J4 PIN		A15J4 PIN	
1	I/O VCC2	26	RP BUX 5
2	I/O VCC2	27	RP BUS 5
3	$\overline{8000}$	28	STROBE X
4	$\overline{100,000}$	29	STROBE RANGE
5	$\overline{100}$	30	TRIGGER
6	$\overline{400}$	31	STROBE MT
7	$\overline{2000}$	32	STROBE REF
8	$\overline{200}$	33	RP BUS 3
9	$\overline{4000}$	34	$\overline{ARM}$
10	$\overline{10}$	35	RP BUS 2
11	$\overline{1000}$	36	I/O Vcc1
12	$\overline{20}$	37	I/O Vcc 1
13	$\overline{40,000}$	38	RP BUS 6
14	$\overline{800}$	39	RP BUS 1
15	$\overline{RANGE\ 3}$	40	I/O GND
16	(NO CONN.)	41	I/O GND
17	$\overline{RANGE\ 2}$	42	$\overline{80000}$
18	$\overline{40}$	43	$\overline{RANGE\ 1}$
19	$\overline{2}$	44	$\overline{20000}$
20	$\overline{1}$	45	$\overline{LOW\ RANGE}$
21	$\overline{RANGE\ 4}$	46	$\overline{OVERLOAD}$
22	(NO CONN.)	47	$\overline{+}$
23	$\overline{8}$	48	$\overline{10,000}$
24	$\overline{4}$	49	$\overline{CONVERT}$
25	$\overline{80}$	50	$\overline{RANGE\ 0}$

NOTE: MATING CONNECTOR AMPHENOL MICRORIBBON 57-30500
OR EQUIVALENT.

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4 CALIBRATION

4.1 GENERAL

Model 7500 DMM is designed to provide in-spec performance for a period of 6 months without recalibration. The calibration should be checked at 6-month intervals, and more frequently if the equipment has been exposed to severe environmental stress. Chapter 4 provides instructions for checking the calibration and for recalibrating when necessary. If the multimeter cannot be adjusted to specified performance, refer to Chapter 7, Maintenance, for additional information.

4.2 TEST STANDARDS & MEASUREMENT INSTRUMENTATION

Table 4-1 lists the test and measuring instruments that are required for calibration procedures. The table includes those standards needed for calibrating the complete Model 7500 DMM, including installed options for ACV, K OHMS, REFAC, and REFDHMS measurement. Calibration and maintenance information for interface options are included as supplements for the particular interface option installed.

> WARNING
>
> Model 7500 DMM parallels front and rear input terminals. Make certain that no connections are made to the other set of terminals before connections are made.
>
> Observe limits as defined in specifications (Chapter 1) on all applied voltages.

4.3 OVERALL PERFORMANCE CHECKS (BASIC 7500)

a. The performance of Model 7500 DMM should be checked before any calibration adjustment is made. Such checks are made simply by using the internal test reference against a known external standard. Turn on power; allow 1 hour to warm up; perform the checks in the sequence that follows. If an out-of-specification performance is obtained, proceed to paragraph 4.5 for the calibrating instructions.

Note: Tests should be conducted at ambient temp. of 23°C ± 5°C: else limits should be corrected for temperature coefficients.

b. Zero Check (DCV)

Place shorting link between X HI and X LO, and GUARD posts.

(1) Operate LOCAL pushbutton for LOCAL control.

(2) Operate INPUT CHANNEL DCV pushbutton.

(3) Operate REF CHANNEL INT REF pushbutton.

(4) Operate RANGE 1 pushbutton.

(5) Adjust trigger control to mid-range position.

(6) Operate CONVERT TIME pushbuttons as shown in table below and verify display values between limits shown in table.

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TABLE 4-1

RECOMMENDED TEST EQUIPMENT

TYPE	SIGNIFICANT REQUIRED CHARACTERISTICS	RECOMMENDED MODELS
DC Voltage Standard	10ppm accuracy with calibration corrections 1μV to 1100V DC settings Low noise and ripple 15μV RMS	Cohu Model 555 Optimation (Julie) Model AC126 with PA226
DC Voltage Standard (secondary)	100μV to 11V DC Good short term stability Low noise and ripple	Analogic Model AN3100
Digital Multimeter	10μV resolution as null indicator Battery operated for very high CMRR	Data Precision Model 248
AC Voltage Standard	Frequency: 20Hz to 100kHz 1mV to 1000V RMS settings Voltage stability: ±0.02% for six months	HP Model 745A with 746A Optimation (Julie) Model AC126 with PA226
Oscillosope Main Frame	50mHz bandwidth or greater Plug-in vertical and horizontal channels	Tektronix 7603
Time Base Plug-In	Delaying sweep, 5nS/div to 5S/div Time Base	Tektronix 7B53A
Differential High Gain Amplifier Plug-In	10μV/div to 10V/div deflection factors Selectable bandwidths DC to 1MHz DC offset, 100000:1 CMRR	Tektronix 7A22
Dual trace Wide Band Amplifier Plug-In	DC to 75MHz bandwidth 5mV/div to 5V/div	Tektronix 7A18
Logic Analyzer Plug-In	16 Channels (Not required for calibration of Model 7500 but very helpful in trouble-shooting, especially of microprocessor options.)	Tektronix 7D01
Probes	X1 and X10 low capacitance types	
Resistance Standards	Decade values 100Ω to 10MΩ and 1900Ω 0.0015% absolute accuracy 4 wire configuration of terminals below 10K	Julie Type NB1
Precision DC Voltage Divider	100:1 ±10ppm division ratio, 10K Z_{in}	Julie Type NB1
Resistor	10 Megohm ±10% composition carbon type	Allen Bradley RC07
Capacitor	0.1μf ±10% Polystyrene film, 50V or more	Arco Type PJ
Cables, shielded	Teflon or Polystyrene low leakage dielectrics, copper - low thermal emf conductors.	
Pulse Generator	0-5V pulses, adjustable rates 0-1KHz	

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4.3.b.(6)

CONVERT TIME	SPEC. LIMITS TOLERANCE
64 ms	± .000004
8 ms	± .000006
1 ms	± .000012

(7) Operate RANGE 10 pushbutton.

(8) Operate CONVERT TIME pushbutton as shown in the table below and verify display values within limits shown in table.

4.3.b.(8)

CONVERT TIME	SPEC. LIMITS TOLERANCE
64 ms	± 00.0002
8 ms	± 00.0003
1 ms	± 00.0006

c. TEST Checks.

Remove shorting link from X input.

(1) Remain in LOCAL control.

(2) Operate INPUT CHANNEL TEST pushbutton.

(3) Operate REF CHANNEL INT REF pushbutton.

(4) Adjust trigger control to mid-range position.

(5) Operate RANGE and CONVERT TIME pushbuttons in the combinations shown in the table below. Verify the display values between limits shown in table.

d. External Test Checks

Apply + 10.0000 volts dc to input terminals.

(1) Remain in LOCAL control.

4.3.c.(5)

RANGE	CONVERT TIME	NOMINAL DISPLAY	SPEC. LIMITS TOLERANCE
.1	X	OVLD	
1	64ms	1.00000	± .00006
	8ms	1.00000	± .00007
	1ms	1.00000	± .00013
10	64ms	01.0000	± .0002
	8ms	01.0000	± .0003
	1ms	01.0000	± .0007
100	64ms	010.000	± .002
	8ms	010.000	± .003
	1ms	010.000	± .007
1K	64ms	0010.00	± .02
	8ms	0010.00	± .03
	1ms	0010.00	± .07

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(2) Operate INPUT CHANNEL DCV pushbutton.

(3) Operate REF CHANNEL INT REF pushbutton.

(4) Adjust trigger control to mid-range position.

(5) Operate RANGE 10 pushbutton.

(6) Operate CONVERT TIME pushbuttons as shown in table below and verify appropriate readings within specified limits.

4.3.d.(6)

CONVERT TIME	SPEC. LIMITS TOLERANCE*
64 ms	± .0006
8 ms	± .0008
1 ms	± .0014

* Nominal = + 10.0000

4.4 OVERALL PERFORMANCE CHECKS (OPTIONS)

For each installed signal conditioning option, apply a known input at approximately full scale corresponding to RANGE 10 and verify that the displayed value is within specified tolerance limits. The table below of displayed values assumes a RANGE 10 input of 19.0000 and indicates the tolerances for the selected CONVERT TIME of 64 ms.

SPEC. TOLERANCE LIMITS

ACV* AC1	ACV* AC2	KOhms
± 0.0106	± 0.0335	± 0.0022

* Nominal input is 19.0000 VRMS at 1 KHz

** Nominal input is 19.0000 Kohms

4.5 CALIBRATION ADJUSTMENTS

a. The calibration adjustments are mounted at the upper edges of the PC board assemblies and are accessible when the Model 7500 DMM top cover and GUARD cover are removed.

CAUTION
Observe care when removing covers. High voltage terminals are exposed when covers are removed.

b. Figure 4.5-1 indicates the locations of the adjustment controls in the guarded analog assemblies, and the adjustments are described in the tables that follow.

c. Module A1, Reference Ohms (RK01 - RK06). Reference DC (RDC01 - RDC05).

Adj	Description
R5	Amplifier Gain (RK01 -RK06, RDC01,RDC02)
R4	Amplifier Gain Balance (RK01 - RK06, RDC01, RDC02) Attenuator Balance 1:(RDC05)
R2	HI Amplifier Zero (RK01 - RK04, RDC01, RDC03)
R50	HI Amplifier Zero (RK05, RK06, RDC02, RDC04)
R7	Lo Amplifier Zero (RK01 - RK04, RDC01, RDC03)
R53	Lo Amplifier Zero (RK05, RK06, RDC02, RDC04) Attenuator Balance 2 (RDC05)
R21	Current Source Amp Zero (RK01 - RK06)
R20	Current Full Scale Adjust.(RK01 - RK06).

d. Module A2, Ohms Signal Conditioning (Option K1)

Adj	Description
R2	10K Current Adj. (0.1 mA)
R4	100K Current Adj. (0.01 mA)
R6	1 MEG Current Adj. (0.001 mA)
R10	10 MEG Current Adj. (0.0001 mA)
R13	1K Current Adj. (1 mA)

e. Module A3, Reference AC Signal Conditioning ((Option RAC01-RAC10)

Adj	Description
C4	Hi Frequency Gain Adj.
R17	Rectifier Zero Balance
R29	Output Offset Zero
R26	Low Frequency Gain Adj.

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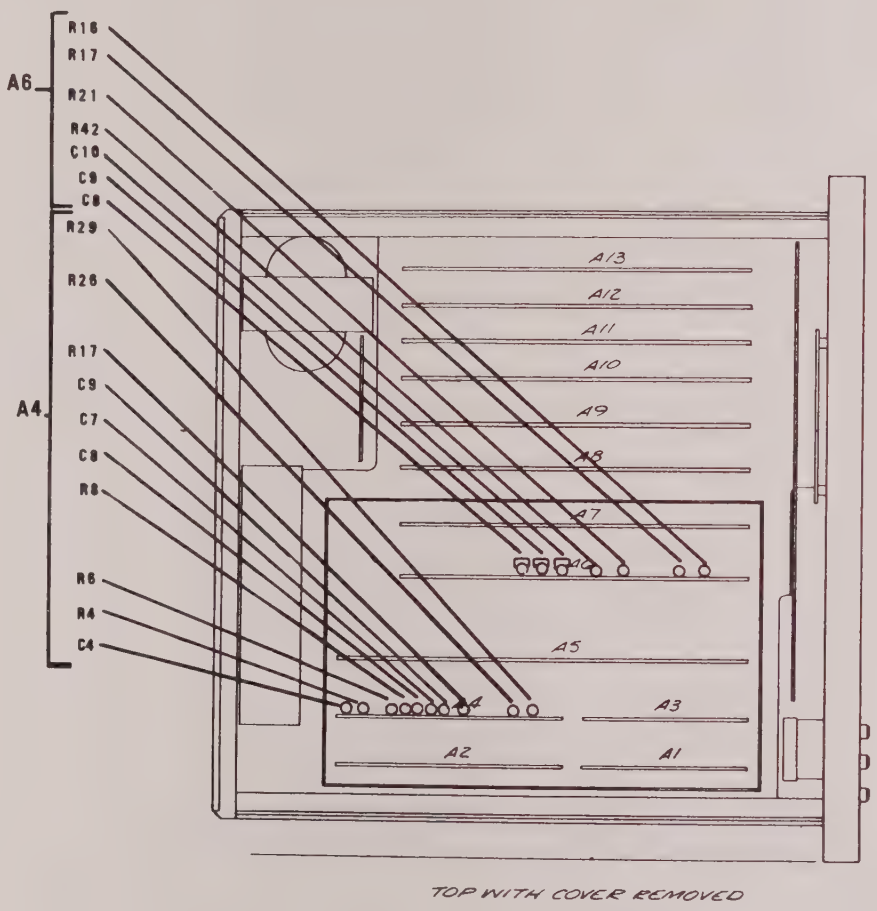

Figure 4.5-1. Location of Calibration Adjustments (Covers removed.)

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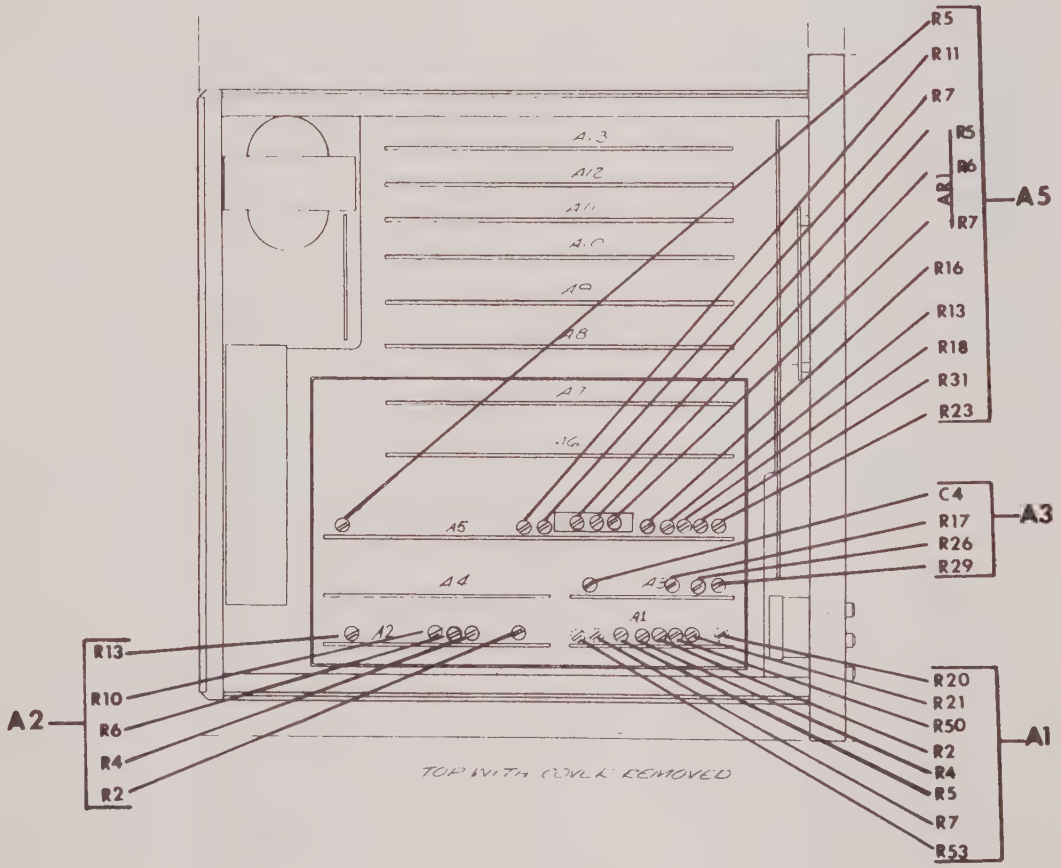

Figure 4.5-1. Location of Calibration Adjustments (Covers removed.)

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f. Module A4, AC Signal Conditioning (AC1,AC2)

Adj	Description
C4	1000V Range HF Gain
C7	100V Range HF Gain
C9	10V Range HF Gain
C8	1V Range HF Gain
R4	100V Range LF Gain
R8	10V Range LF Gain
R6	1V Range LF Gain
R26	1000V Range LF Gain
R17	Rectifier Zero Balance
R29	Output Offset Zero

g. Module A5, DC Signal Conditioning

Adj	Description
AR1 R5	Voltage Zero
AR1 R6	Current Zero
AR1 R7	Second Stage Voltage Zero
R5	100V DC Gain
R7	1V DC Gain
R11	0.1V DC Gain
R18	EXT DC REF Zero
R13	EXT DC REF Gain Hi
R16	EXT DC REF Gain CMRR (LO)
R23	INT REF Adjust
R31	1V Test Adjust

h. Module A6, A/D Analog

Adj	Description
R16	10V DC + Gain
R17	10 DC - Gain (+/- Balance)
R21	Fast Sw. Transient Cancellation (Diff)
R42	Auto Zero Sw. Transient Cancellation
C8	PLUS SLOW Charge Balance
C9	Fast Sw. Transient Cancellation
C10	Slow Sw. Transient Cancellation

4.6 RECALIBRATION SEQUENCE

a. When the results of the performance checks of the previous paragraphs indicate the need for recalibrating Model 7500 DMM, follow the sequence of operations shown in Figure 4.6-1. As shown in the illustration, the Basic Model 7500 is recalibrated first in a prescribed sequence, and then the installed option modules are recalibrated.

b. In brief, the recalibration of the Basic Model 7500 DMM configuration establishes accurate references of -10V and -1V, adjusts for possible transient disturbances that may result from the phase switching actions, trims the divider networks for accurate DCV measurements on the different ranges, and, finally, sets the gain and CMRR of the external reference conditioning amplifier.

4.7 DCV RECALIBRATION (Fig. 4.7-1)

4.7.1 AMPLIFIER ZERO CHECK

a. Select RANGE .1, DCV INPUT CHANNEL, INT REF, 64ms CONVERT TIME, FILTER IN and a convenient TRIGGER RATE for viewing. Allow 1 hour for warmup time with covers in place before making any adjustments.

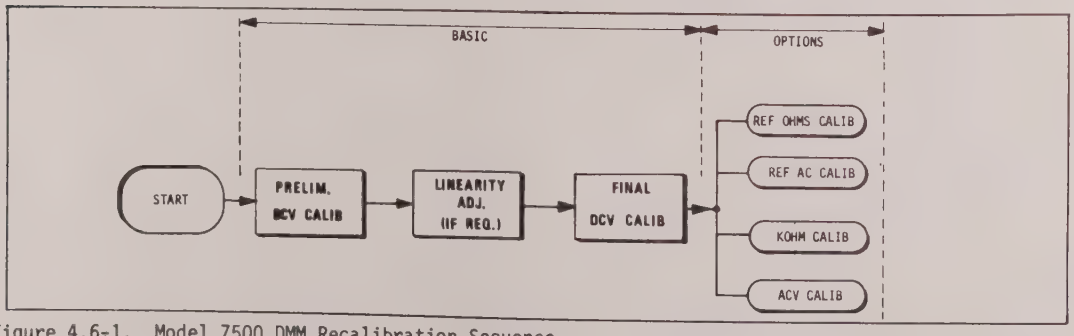

Figure 4.6-1. Model 7500 DMM Recalibration Sequence

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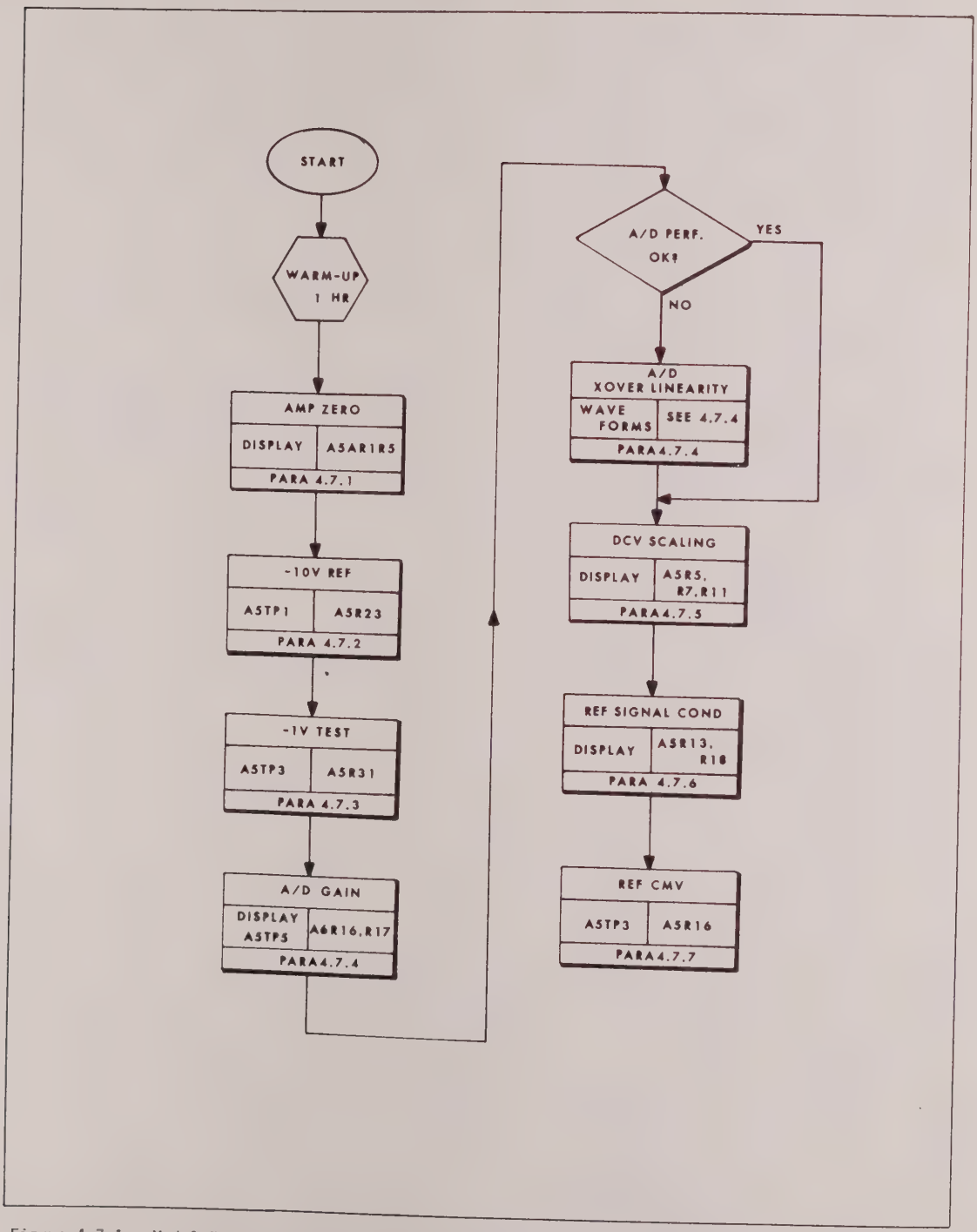

Figure 4.7-1. Model 7500 DMM DCV Recalibration sequence. (Assembly Module A5)

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Connect X HI to X LO with parallel combination of 10 Megohm resistor, carbon type and 0.1µf polystyrene capacitor.

b. Connect X HI to X LO with low thermal EMF banana plug shorting link at front panel binding posts.

c. Check display. If not ±.000000 to ±.000001, adjust R5 in A5 AR1 for display that flickers equally between plus and minus zero.

d. Select FILTER OUT. Remove shorting link.

e. Check display. If not ±.000000 to ±.000050, adjust R6 in A5 AR1. (Allow for 10 second settling time between adjustments.)

f. Repeat steps b, c, d, and e above until the adjustment of R5 and R6 result in the specified display values. Attempt to minimize the effects of thermal transients during this step of the procedure by removing the covers only while making the adjustments.

g. Steps c and e have assumed that the meter A/D converter is only slightly out of calibration near zero and can be used for null indication. Otherwise, use a high input impedance voltmeter (Data Precision Model 248) capable of measuring below 50 microvolts DC at null. Connect it between A5TP5 (REF. RET.) and A5TP4 (VIN. COND.). Allow 100 microvolts indicated by the external voltmeter for each least significant digit count in the adjustment procedure using the display above. If grossly unstable readings are obtained using the external voltmeter, check the test circuit for AR1 oscillations due to excessive voltmeter input capacitance, noise or ground loops. Each 100 microvolts of off null indication represents 1µV referred to the input of AR1 with input shorted, or 0.1pA of input current with 10 Megohms source impedance.

4.7.2 -10V REFERENCE ADJUSTMENT

a. Connect voltage standard, Model 248 DMM and Model 7500 DMM A5TP1 as shown in Figure 4.7.2-1.

b. Adjust the standard for an output of 10.00000V. (-10V relative to X LO.)

c. Adjust A5R23 in Model 7500 DMM for null (±00.00) reading on the Model 248 DMM (100mV range).

4.7.3 -1V REFERENCE ADJUSTMENT

a. Reconnect Model 248 DMM HI to Model 7500 DMM A5TP2.

b. Adjust the standard for an output of 1.000000V.

c. Adjust A5R31 in Model 7500 DMM for null (±00.00) reading on Model 248 DMM (100mV range).

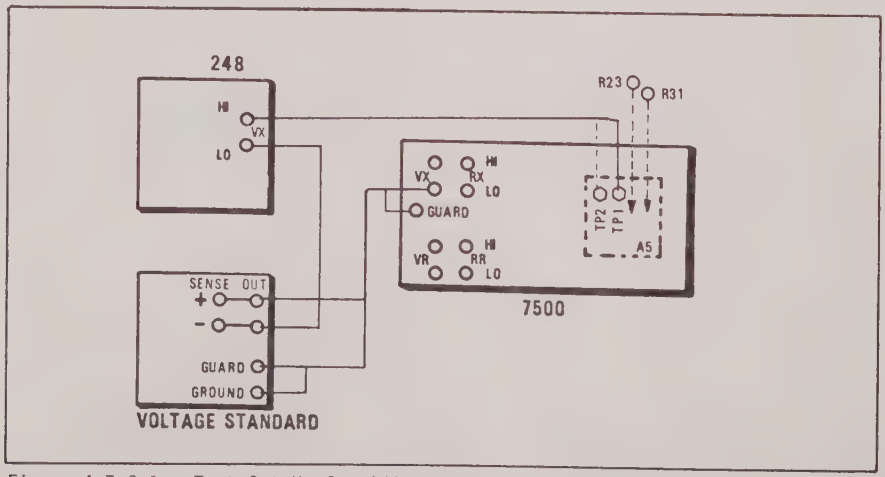

Figure 4.7.2-1. Test Set Up for Adjusting A5R23, A5R31

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4.7.4 A/D GAIN AND CROSSOVER LINEARITY ADJUSTMENTS

a. Select DCV, INT REF, 10V RANGE, 64 ms CONVERT TIME, FILTER IN, EXT RATE to a convenient rate. Connect DC Voltage Standard as shown in Figure 4.7.4-1.

b. Set DC standard to input +19.00000V.

c. Adjust A6R16 for reading of +19.0000.

d. Set or reconnect DC standard to input -19.00000V.

e. Adjust A6R17 for reading of -19.0000V.

* * * * * * * * * * * * * * * * * * * *
*
* WARNING: The following adjust- *
* ments require the use of an *
* ungrounded oscilloscope. Check *
* for the absence of hazardous *
* voltages before touching any *
* metallic portions of the oscillo- *
* scope or associated probes. *
*
* * * * * * * * * * * * * * * * * * * *

NOTE: The following linearity adjustments should not be performed unless the A/D converter exhibits one or more of the following symptoms on the 1 millisecond Convert Time: (1) Missing code values in one or both polarities near zero; (2) Wide zero code of more than 2 counts value; (3) Linearity discontinuity (missing or more than 2 count wide codes) at dual/triple slope transition located between 300 and 500 counts in either polarity; (4) Code trapping where input values in a band several counts wide below a code ending in 00 all result in display of the code ending in 00. Be sure your test equipment is adequate before attempting any adjustment. Factory selected components should not require any change unless other related components have been replaced.

f. Set EXT RATE to EXT position. Connect Pulse Generator and Oscilloscope with High Gain Preamp and Time Base Plug-ins as shown in Figure 4.7.4-1.

f. Select 1ms CONVERT TIME, set DC Standard to -0.002000V, connect oscilloscope for external triggering and adjust Pulse Generator to trigger both the Model 7500 and the Oscilloscope at about 100Hz. Set the Oscilloscope for 50μS/div., 1mV/div., DC to 300 KHz bandwidth. Connect probe to A6TP5 and adjust vertical positioning and DC offset controls to bring the trace on screen.

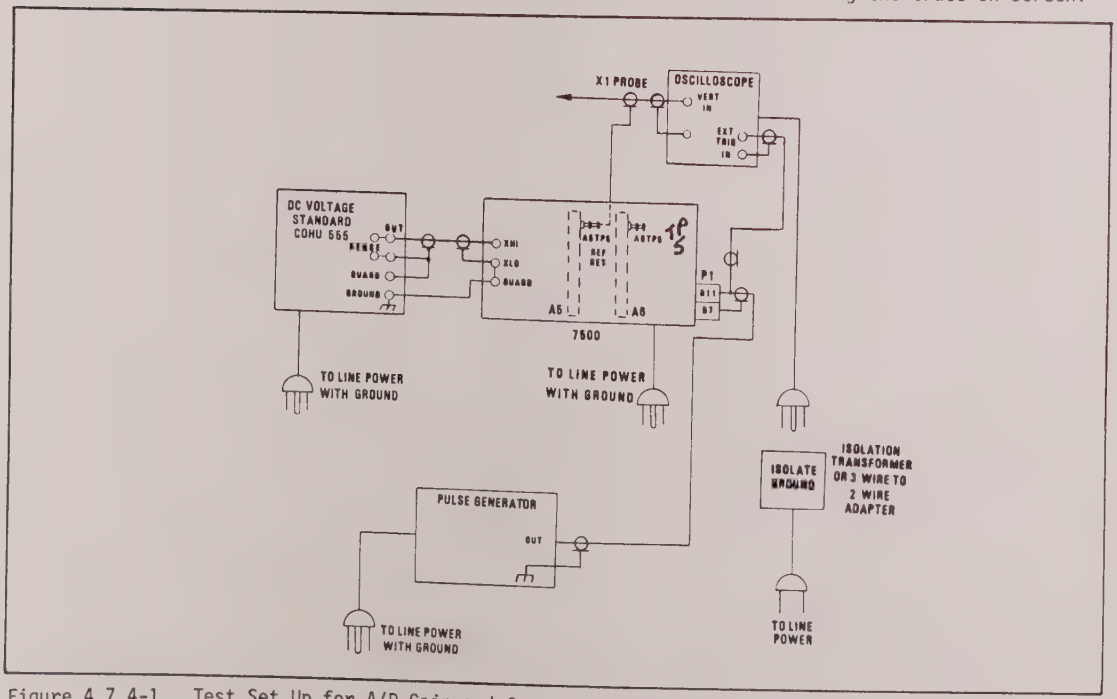

Figure 4.7.4-1. Test Set Up for A/D Gain and Crossover Linearity Adjustments

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g. Refer to Figure 4.7.4-2 for locations of lettered points on waveforms. Adjust A6R21 such that the level of the second pause, D, matches the level at the end of the input integration, C. Note that adjustment of A6R21 will move both levels A and D.

h. Adjust A6C9 such that the level of the first pause, A, matches the level at the beginning of input integration, B. Repeat step g. and this one until both A matches B and C matches D. If the adjustment cannot be brought into range, FSV A6C13 may require a change of value.

i. Adjust A6R42 to match the autozero level, F, with the level of the first pause, A. If this adjustment is out of range, FSV A6 C30 may require a change of value.

j. Check zero balance. Remove probe from A6TP5, select 64ms CONVERT TIME, and internally trigger the Model 7500 at a slow rate. Input plus 1mV and minus 1mV from the standard and observe the readings of the Model 7500. The balance should be within 1 count centered at ±10 counts. For example, if -1mV input reads flickering between -9 and -10 counts, then +1mV should read no more than +10 flickering to +11 counts. If careful adjustment of the preceeding steps does not result in adequate balance, FSV A6 R33 may require a change of value. Any gross imbalance indicates a failed component such as a defective FET switch.

k. Repeat steps b, c, d, and e with scope probe disconnected.

l. Check midrange balance. Input +10.00000 volts and observe reading error, then input -10.00000 volts and observe reading error. Balance should be no worse than 9.9999 in one polarity and 10.0001 in the other polarity. FSV R22 affects this balance, since reducing R22 resistance raises the count at -10V and lowers the count at +10V, but a gross imbalance indicates some failed component problem.

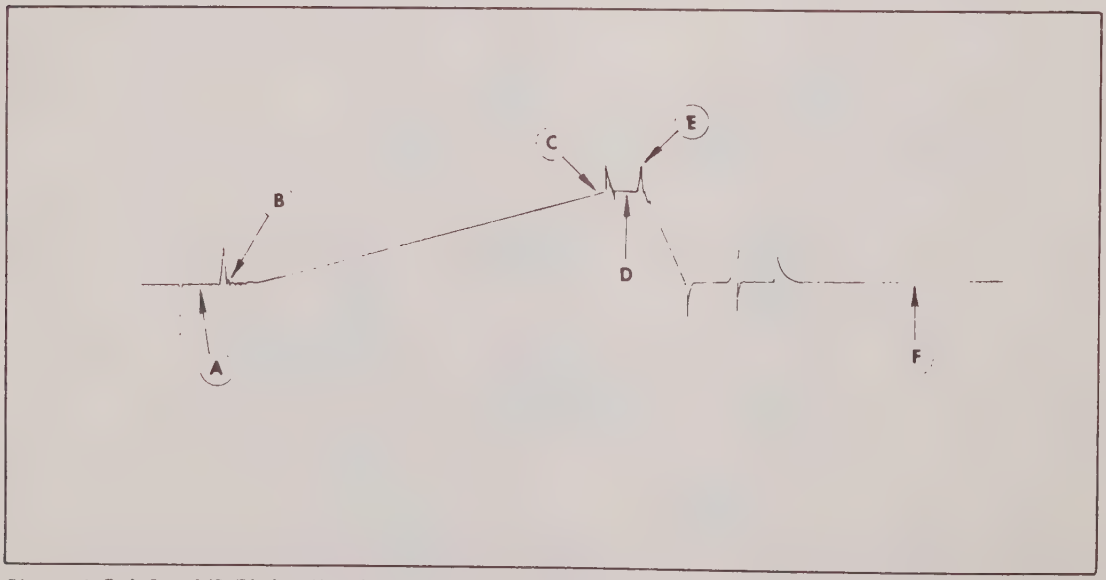

Figure 4.7.4-2. A/D Timing Waveforms. Scope at 1mV/Div.

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m. Select 1ms CONVERT TIME, EXT TRIGGER. Reconnect the oscilloscope probe to A6TP5. Set the scope gain to 100μV/div and bandwidth to DC to 100KHz. Set the voltage standard to -1mV. Refer to Figure 4.7.4-3. Adjust the scope DC offset and use the delayed sweep to bring the waveform area being adjusted on screen.

n. Readjust A6R21 slightly if required as in step g. such that C and D match within 20μV.

o. Readjust A6C9 slightly if required as in step h. such that A and B match within 20μV.

p. Find level F by slowing sweep to 0.5ms/div. and lowering bandwidth to 30KHz. Return scope to 100KHz and 50μS/div. Adjust A6R42 such that A matches F within 30μV.

q. Remove all scope and trigger pulse connections to the Model 7500. Select a slow internal trigger RATE. With input of -0.001000V adjust A6 C10 for a reading of -0.0010V. The amplitude of spike, E, on the waveform, Figure 4.7.7-3, is adjusted by C10. FSV A6 C14 and W2 center the range of adjustment of C10. This adjustment is influenced by the source to gate capacitance of A6 Q17 so replacement of Q17 may require reselection of the FSV.

r. With an input of +0.001000V adjust A6 C8 for a reading of +0.0010V. FSV A6 C11 and W1 center the adjustment range of C8, if required.

s. Check gain and linearity at ±19.9988V, ±19.0000, ±10.0000, ±0.0500, ±0.0010 and 0.0000 for each CONVERT TIME. See Table at end of chapter.

4.7.5 DCV SCALING ADJUSTMENTS

a. Select DCV INPUT CHANNEL, INT REF, REF CHANNEL, RANGE 10, 64ms CONVERT TIME, FILTER IN, and TRIGGER RATE at mid-range.

b. Connect voltage standard to Model 7500 DMM as shown in Figure 2.2.

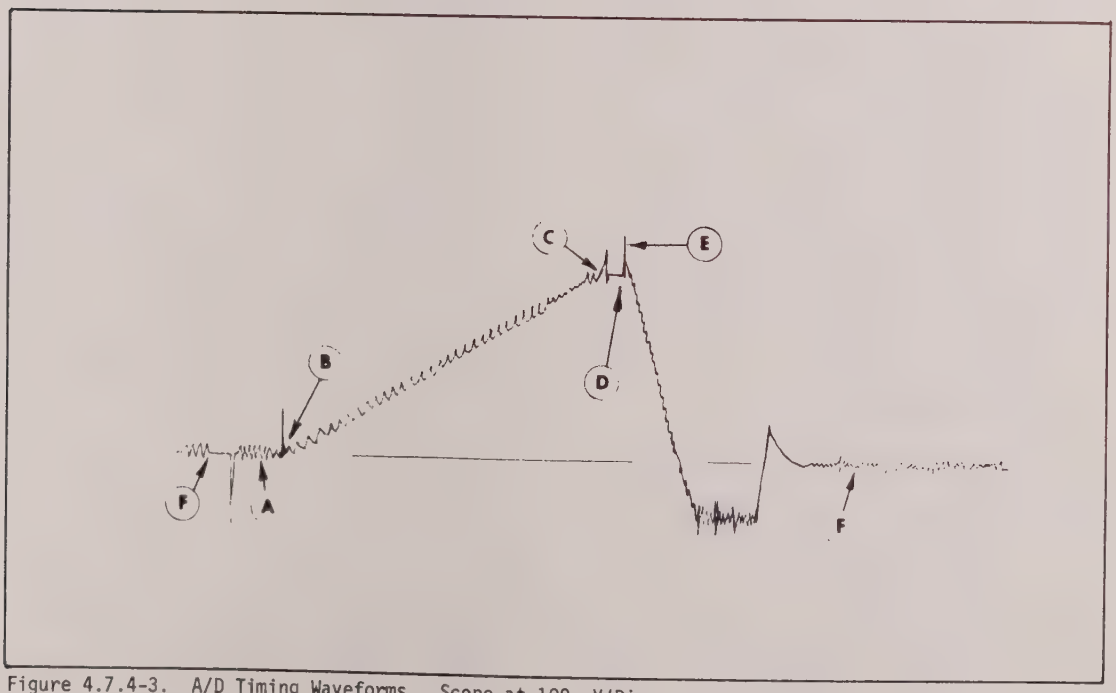

Figure 4.7.4-3. A/D Timing Waveforms. Scope at 100 μV/Div.

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c. Select RANGE 100 on Model 7500 DMM.

d. Adjust voltage standard for +190.000V output.

e. Check Model 7500 DMM display. Adjust A5R5 for reading of +190.000 on display.

f. Adjust voltage standard for +1.90000V output.

g. Select RANGE 1 on Model 7500 DMM.

h. Check Model 7500 DMM display. Adjust A5R7 for +1.90000 on display.

i. Adjust voltage standard for +0.190000V output. NOTE: If the noise component of the standard's output is excessive on this range, use the standard set at 19.0000V to drive a 100:1 precision voltage divider and connect its divided output to the Model 7500.

j. Select RANGE .1 on Model 7500 DMM.

k. Check Model 7500 DMM display. Adjust A5R11 for +.190000 on display.

l. If display value is .190000 +.000006, proceed to para 4.7.5. If incorrect value is displayed, repeat steps h through l.

4.7.6 REFERENCE SIGNAL CONDITIONING ADJUSTMENTS

a. Connect inputs at Model 7500 DMM and Model 3500 DMM as shown in Figure 4.7.6-1.

b. Adjust A5R18 for null as measured by Model 3500 DMM (.1 range scale).

c. Connect voltage standard inputs to model 7500 DMM as shown in Figure 4.7.6-2

d. Select TEST INPUT CHANNEL, RANGE 1, CONVERT TIME of 64ms, and trigger RATE at mid-range.

e. Adjust voltage standard for +10.0000V output.

f. Alternately, select INT REF and DC as the REF CHANNEL and read display. Adjust A5R13 for exactly equal display value.

4.7.7 REFERENCE COMMON MODE ADJUSTMENTS

a. Connect voltage standard, Model 7500 DMM and Model 3500 DMM as shown in Figure 4.7.7-1.

b. Select DC REFERENCE CHANNEL on Model 7500 DMM.

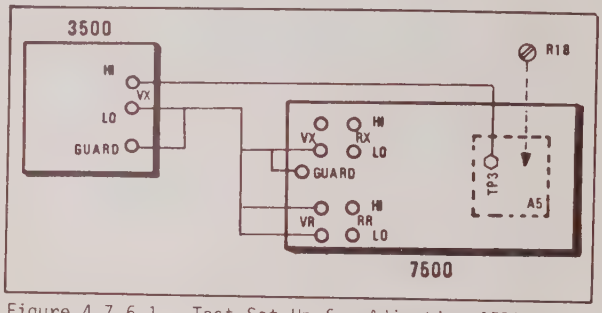

Figure 4.7.6-1. Test Set Up for Adjusting A5R18

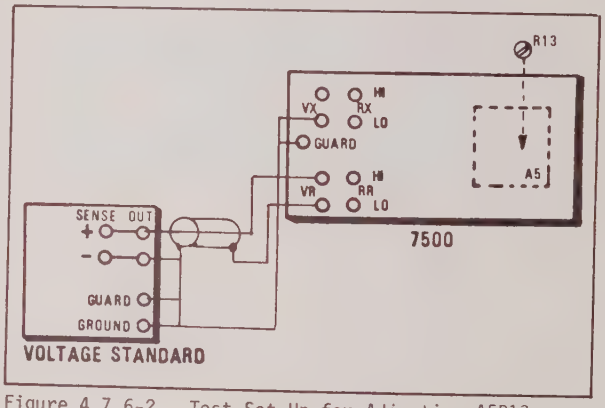

Figure 4.7.6-2. Test Set Up for Adjusting A5R13

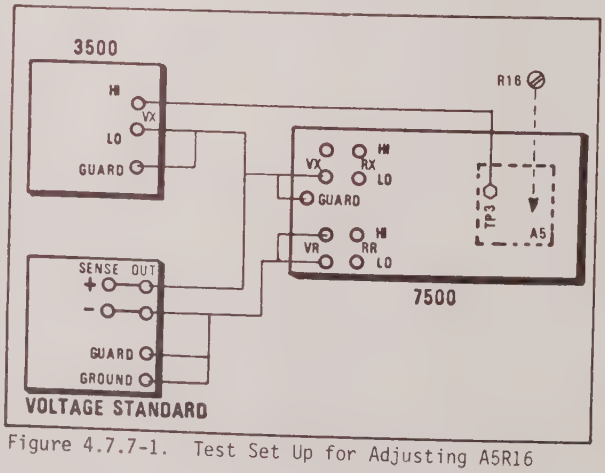

Figure 4.7.7-1. Test Set Up for Adjusting A5R16

c. Set voltage standard to zero and to ±10 volts DC, and note voltage output at TP3 as indicated by reading on Model 3500 DMM (.1 range). Adjust A5R16 to minimize the peak excursion from a null reading at the 3 voltage standard settings.

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4.7.8 REFERENCE LIMITS COMMON MODE CHECK

a. Connect Model 7500 DMM as shown in Figure 4.7.8-1.

b. Select TEST INPUT CHANNEL, DC REF CHANNEL, 64ms CONVERT TIME, and mid-range trigger RATE.

c. Adjust Reference Voltage Generator to +11V.

d. Adjust CMV generator to 0V. Record value.

e. Adjust CMV generator to +10V. Record value.

f. Adjust CMV generator to -10V. Record value.

g. Adjust Reference Voltage to -11V, and repeat steps d, e and f above.

h. Proper operation of Model 7500 DMM is indicated if recorded values for CMV = ±10V are within 2 counts of the value at CMV = 0V. If not, return to paragraph 4.7.6 and repeat calibration.

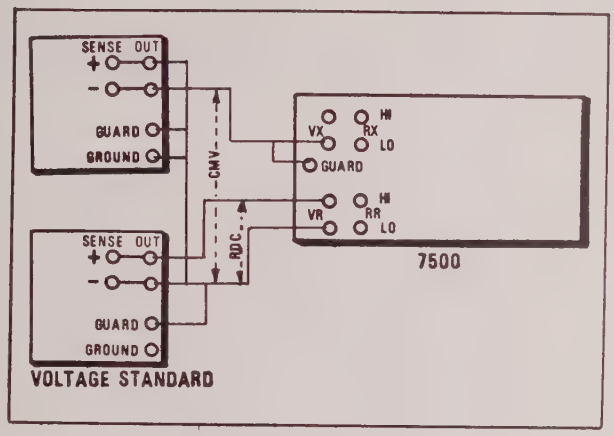

Figure 4.7.8-1. Test Set Up for Checking Reference Limits Common Mode

4.7.9 THERMAL EFFECT CHECK

a. Install all covers and allow 1 hour warmup.

b. Check .1 Range zero as in steps 4.7.1, subparagraphs a through f. Readjust A5AR1R5 if required.

c. If step b above required readjustment at zero, check and readjust .1 Range full scale as in step 4.7.5 subparagraphs i through l.

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TABLE OF INITIAL LINEARITY LIMITS
(Refer Paragraph 4.7.4s)

DC INPUT VOLTAGE RANGE10	CONVERT TIME					
	1ms		8ms		64ms	
	HIGH	LOW	HIGH	LOW	HIGH	LOW
+19.9988	OVLD	+19.9970	+19.9999	+19.9977	+19.9998	+19.9978
+19.0000	+19.0017	+18.9983	+19.0011	+18.9989	+19.0010	+18.9990
+10.0000	+10.0012	+9.9988	+10.0007	+9.9993	+10.0006	+9.9994
+0.0500	+0.0506	+0.0494	+0.0503	+0.0497	+0.0502	+0.0498
+0.0010	+0.0016	+0.0004	+0.0013	+0.0007	+0.0012	+0.0008
0.0000	+0.0006	-0.0006	+0.0003	-0.0003	+0.0002	-0.0002
-0.0010	-0.0004	-0.0016	-0.0007	-0.0013	-0.0008	-0.0012
-0.0500	-0.0494	-0.0506	-0.0497	-0.0503	-0.0498	-0.0502
-10.0000	-9.9988	-10.0012	-9.9993	-10.0007	-9.9994	-10.0006
-19.0000	-18.9983	-19.0017	-18.9989	-19.0011	-18.9990	-19.0010
-19.9988	-19.9970	OVLD	-19.0077	-19.9999	-19.9978	-19.9998

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5 SYSTEM OPERATION

5.1 INTRODUCTION, CHAPTER OVERVIEW

Chapter 5 presents an explanation of Model 7500 operation in terms of its functional subsystems. Detailed DMM 7500 circuit implementation of these functions is explained in Chapter 6. The descriptions in Chapter 5 are centered about two flow diagrams: Figure 5-1 defines the logical flow, while Figure 5-3 defines the interrelationships among physical/functional modules in terms of one-line control and data signals connecting them.

5.2 SYSTEM FLOW LOGIC (Fig. 5-1)

As shown in figure 5-1, turning on DMM 7500 power enables two parallel logic flows: a program control logic section, and an analog-to-digital conversion logic cycle. The interrelation between these two logic sections is indicated in figure 5-1 by the circled letters indicating "states" established by the program control logic and the corresponding decision points in the conversion logic where the program logic "state" determines the subsequent logic path. Some of the conversion decision points require the results of prior conversion events, and these are implicit in the conversion flow.

5.3 PROGRAM CONTROL LOGIC FLOW

5.3.1 Default Functions.

In the absence of any signal to the contrary, upon application of power, the DMM 7500 will select the following conversion control configuration:

Measurand: DC voltage (DCV) Signal Conditioning

Reference: Internal (INT)

Measurement Time: 64 milliseconds (64ms)

Remote/Local Control: LOCAL

5.3.2 Control.

a. The first decision determines the source of program control: either rear (Remote) or front panel (Local) inputs. If REMOTE control has been selected by the user, the DMM enables the remote programming of 6 bus lines. Where program control is REMOTE, the states of the 6 remote programming bus lines may be strobed into registers from which the conversion cycle and function control levels will be transmitted. If the source of program control is LOCAL, the setting of the front panel controls establish the control levels latched into the registers. In REMOTE program control, the conversion start signal which is the normal output of the program control logic is inhibited for 40 milliseconds, when any change of control settings is initiated. During this delay, the PROG BUSY flag is set, transmitting an indication to allow for completion of the programming changes prior to start of conversion cycle.

b. In LOCAL control, conversion control signals are generated as determined by the front panel trigger rate control setting.

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5.4 A/D CONVERSION CONTROL LOGIC FLOW

5.4.1 Trigger.

a. Each conversion cycle is initiated by a trigger control signal that is generated either by DMM 7500 circuitry or by connection to a remote source, as determined by the setting of the front panel EXT-RATE switch D. In its ccw position, the switch selects the external source of trigger control, and if none is transmitted, the EXT position holds the display.

b. The DMM 7500 also requires an enabling low signal or open circuit on the $\overline{\text{ARM}}$ line. Then, if the $\overline{\text{PROG BUSY}}$ flag is not active, the measuring phase of the conversion cycle is started. As shown in figure 5-1, the program status signal A establishes the $\overline{\text{PROG BUSY}}$ condition; internal DMM circuitry controls the minimal auto-zeroing time interval.

5.4.2 Phase 2, Integrating the Measurand.

a. After a 16 usec pause, during which the circuits for connecting the selected measurand signal conditioner to the A/D input are able to settle and switching transients die out, the measurand is integrated for 1000 counts of a clock interval determined by the conversion cycle measurement time previously selected: 64 msec, 8 msec, or 1 msec for 60 Hz powering (80 msec, 10 msec, and 1.2 msec for 50 Hz powering of Model 7500 E). During Phase 2 the 1000 counts are accumulated beginning with the 3rd decade of the counter. Thus, with respect to unity decade, the counter has an indicated value of 100000 when the 1000 counts are complete.

b. At the end of the Phase 2 measurand integration, the circuitry senses the polarity of the measurand in order to determine the appropriate polarity of the reference for integration during Phases 3 and 4.

5.4.3 Phase 3, Integrating the Reference (Fast Slope).

A pause of 16 microseconds is initiated at the start of Phase 3 in order to provide settling time for the reference switching circuits and the comparator prior to the integration action during Phases 3 and 4. If the measurand value exceeds a threshold of 0.15% (approx.) of full scale, then integration of the reference begins discharging the capacitor at a fast rate while the counter is incremented at a rate equal to 100 times the least significant bit. This action constitutes Phase 3, and it continues until the charge on the integrating capacitor is reduced to 0.15% of the maximum inrange value. If the signal should exceed the maximum for the selected range, the charge may not be reduced to the 0.15% level; the conversion cycle logic is advanced as discussed later.

5.4.4 Phase 4, Integrating the Reference (Slow).

a. When the threshold value is sensed by the comparator circuit, the integrator discharge current is switched so that the integrating rate is "slow", while the digitizing counter is incremented at the same rate while the input is connected to the least significant bit instead of to the third decade. The "Slow" rate charging current is obtained by dividing the fast-rate reference current by 100, and this operation proceeds until the integrator capacitor charge is reduced to zero. The slow reference integration constitutes Phase 4, and continues until the capacitor zero value is sensed at the comparator.

b. If zero is not reached before the 200000 counter value, the logic flow is advanced as described in para. 5.4.5, following. When either a zero transition or out-of-range condition terminates Phase 4, the value stored in the main counter is transferred to the shift register as the digitized result of that conversion cycle.

5.4.5 Escape Actions in Phase 3 and Phase 4.

a. If the count should exceed full scale, Phases 3 and 4 are terminated and the operation initiates a pause preceding auto-zeroing Phase 1.

b. In normal operation no more than 400 counts should be accumulated during Phase 4 action. However, it is possible that noise may cause a shift to Phase 4 action prematurely. As a result, although the final digitizing count through the end of Phase 4 would probably not be in error, the conversion cycle time may be excessive and would not support a desired high conversion rate. The DMM 7500 includes circuitry to sense an 800 count during Phase 4 action, and if that value is exceeded, the circuitry reintroduces a fast count until the count reaches its maximum value of 240000.

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5.4.6 Phase 1, Auto-Zeroing the Analog Circuitry.

a. Phase 1 is initiated after Pause #3 (of 16 useconds) when either the comparator output is zero (for in-range measurand values), or a value exceeding full scale range is accumulated in the digitizing counter. During this pause, the data transfer logic is actuated. If a 1ms measurement time has been selected, the DMM 7500 initiates a "FAST AUTO-ZERO" to eliminate any analog inter-conversion drifts within the short recovery time available. As shown in figure 5-1, programmed measurement time is an input B from the program status registers.

b. If DMM 7500 was not placed in auto-ranging mode of operation, as indicated by the program status letter C, then the fast auto-zeroing action is concluded after a predetermined time, and the slow auto-zeroing action continues at least until the main counter indicates 240000 (2400 counts), thus providing at least 400 counts of auto-zeroing action before the next conversion is initiated; longer auto-zeroing times are obtained when the value is less than the 200000 full scale value, or when conversions are not triggered at the maximum rate.

c. When the counter indicates 240000 (and no auto-ranging has been selected), the measurand value in the digitizing counter is latched into the display registers and updates the displayed value. The conversion cycle is completed, and the valid data indication is transmitted as negative going transition of CONVERT. Autozero, Phase 1, continues until another trigger starts a new cycle.

5.4.7 Auto-Ranging.

a. If the program status letter C indicates selected auto-ranging mode of operation, the actions of Phase 1 (auto-zeroing) proceed while the data in the shift register for the current conversion cycle is assessed in terms of the present range, and a new range is selected, if appropriate, for the next conversion. CONVERTING remains active until an in-range conversion cycle is complete.

b. As shown in figure 5-1, the selection of auto-ranging mode causes the DMM 7500 to examine the digitized value and to determine if RANGE is OK. If the magnitude is not out-of-range (greater than 199999), or if it is greater than 10% of the selected full scale range (9999), the range is considered OK, and Phase 1 continues as described immediately preceding.

c. If in Auto-Range mode, the digitized value and operable range do not meet the conditions for in-range as defined above, then DMM 7500 initiates an auto-range delay to enable the relay-operated ranging circuits to settle.

d. If the digitized value exceeds the selected full scale range, then the auto-ranging action selects maximum range (Range 1K for voltage and voltage ratio, Range 10K for resistance).

e. If the digitized value is less than 10% of selected full scale range, then ranging counter is decremented to the range that produces the fewest number of leading zero's down to and including the minimum range available. As shown in figure 5-1, the range counter is stepped down 1 range decade at a time, and the resulting digitized value after each step evaluated in terms of leading zero's until no further down-ranging is possible. Eliminating leading zero's or reaching minimum range ends the down-ranging action, and the control signal enabling a new conversion cycle is generated when the auto-ranging delay is completed.

f. It should be noted that the appropriate range will be selected in auto-range after no more than one additional conversion following the out-of-range conversion. This additional cycle occurs if the selected range is too low and the value is greater than full scale range. For, if the present range is too high (greater than 10 times the value), then the auto-ranging circuits will locate the proper range prior to the next conversion.

5.4.8 System Timing Diagram (Figure 5-2).

The timing waveform sequences of figure 5-2 illustrate the relationships identified and discussed with respect to the logic flow chart above. Figure 5-2A illustrates the relationships for an in-range measurand, while figure 5-2B illustrates the differences for an out-of-range (beyond full scale range) input.

5.5 ONE-LINE BLOCK DIAGRAM (Fig. 5-3)

5.5.1 Overview.

a. Architecture of the 7500 DMM essentially allocates functional circuitry to a single module assembly. Thus, as shown in figure 5-3, the functionally designed blocks correspond to physical modules, and meaningful one-line program, control, and data signals connect the functional blocks.

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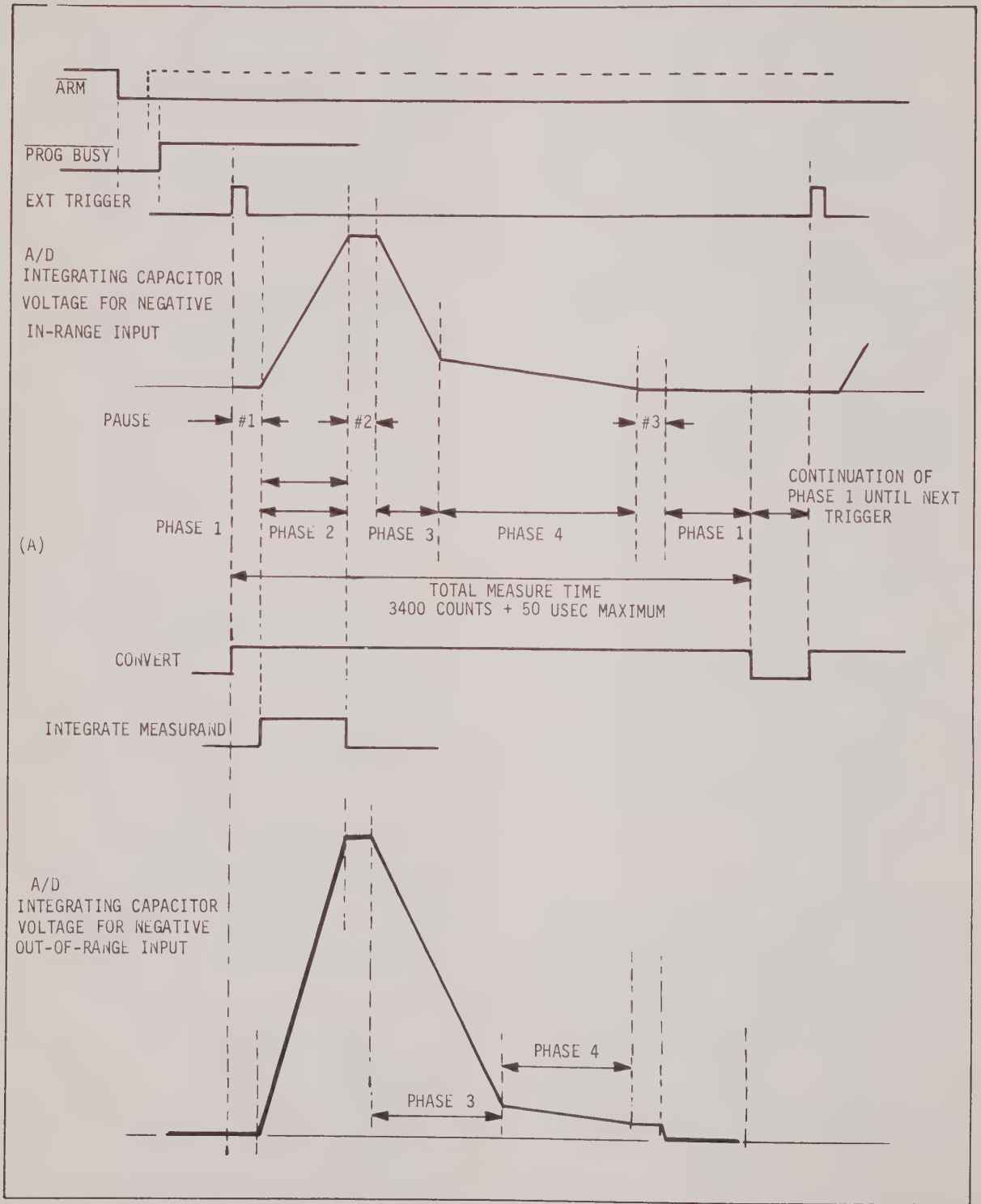

Figure 5-2. Timing Waveforms. (a) In-Range negative input. (b) Out-of-Range negative input.

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b. In brief, the A/D conversion operates on a conditioned dc voltage input and a conditioned dc reference input transmitted by the standard DC Signal Conditioner, Module A5. All other measurands and references are preconditioned by optional assemblies to dc values which may be further conditioned through the DC signal conditioner so that 10 volts at the input to the A/D converter corresponds to nominal range (counter = 100000). Note: Full scale (100% overrange) corresponds to counter= 199999 and 19.9999 volts.

c. Note, also, that analog function modules are indicated as guard-shielded from the other circuitry, and that control and program signals interfacing with the analog circuitry are transmitted and received via relays, transformers, or opto-isolators.

5.5.2 System Control & Program.

a. The conversion proceeds under control of the program stored in the registers of PROGRAM & STATUS assembly A12 and in RANGE & CONTROL assembly A13. These registers are set either by switch inputs at the front panel, or by strobed inputs from the standard interface connector at the rear panel, or by signals from any one of several optional interface controllers. Control of the programmed operations may be exercised in groups so that some or all functions may be controlled only through remote controllers while the remaining may be controlled either at the front panel switches or by remote controllers. In all instances, the results of front panel selected program or remote control selected program are displayed on the appropriate lighted switches of the front panel, assembly A14. These lights indicate selected measurand, selected reference, selected range, auto-range if applicable, and selected measurement time. Conversion rate is not indicated by lights.

b. Inputs from remote controllers are interpreted according to appropriate protocols (refer to Chapter 3), and the decoded selections are set in the appropriate registers of A12 and A13 via the standard interface bus and strobe lines. Voltage levels at these register outputs, in conjunction with internal A/D programming, control the conversion cycle.

5.5.3 Measurand & Reference Inputs.

a. Model 7500 DMM measurement is essentially a ratio measurement of measurand to reference. The measurand is connected to front panel binding posts (HI and LO) or to a rear connector whose terminals are connected in parallel to the front panel. The input is connected to an ac signal condition option (if installed and if selected) via DC Signal Conditioner . The measurand may also be a precision test signal, developed from the internal reference and connected to the DC Signal Conditioner when selecting TEST function.

b. The 7500 DMM enables the user to establish the numerator and denominator independently for the ratiometric conversion. Thus, for example, dc volts may be measured with respect to ohms, or ac volts (if ohms or ac reference options are installed) or with respect to an internal dc voltage standard of 10 volts, as well as with respect to another external dc reference.

c. The basic Model 7500 DMM is configured to accept dc voltage measurands and to digitize the input by using a precision internal reference, and to display the data in 5 1/2 digits with sign and decimal point direct-reading voltage. Operation of the equipment for optional measurands and references is described after the flow description for dc inputs.

5.5.4 DC Signal Conditioning.

a. Measurand inputs, XHI and XLO, are connected to A5, where they are scaled according to the selected range. Figure 5-4 is a simplified schematic of the fundamental operation of A5 in scaling the measurand. As shown in figure 5-4, the input to A5 may be attenuated by a relay controlled voltage divider at the input to amplifier A5AR1, and amplified as determined by the relay-controlled feedback divider network from output to input of AR1 depending upon the selected range. The attenuation - amplification factors are combined so that the output of A5 will be a dc signal, VIN COND, scaled so that 10 volts magnitude will result in 100000 on the display. The selected range also positions the decimal point in the display so that the result may read directly in volts. Figure 5-4 also includes the filter block, which may be switched into the circuit by the front panel or remote control program when in DC Signal Conditioning.

b. Reference input, REF, if internal, is developed in the DC Signal Conditioner, assembly A5, and connected to the A/D converter for use during Phases 3 and 4, under A/D program control. The REF is a precision -10V signal, derived in an active circuit incorporating an oven-controlled thermally stable reference zener.

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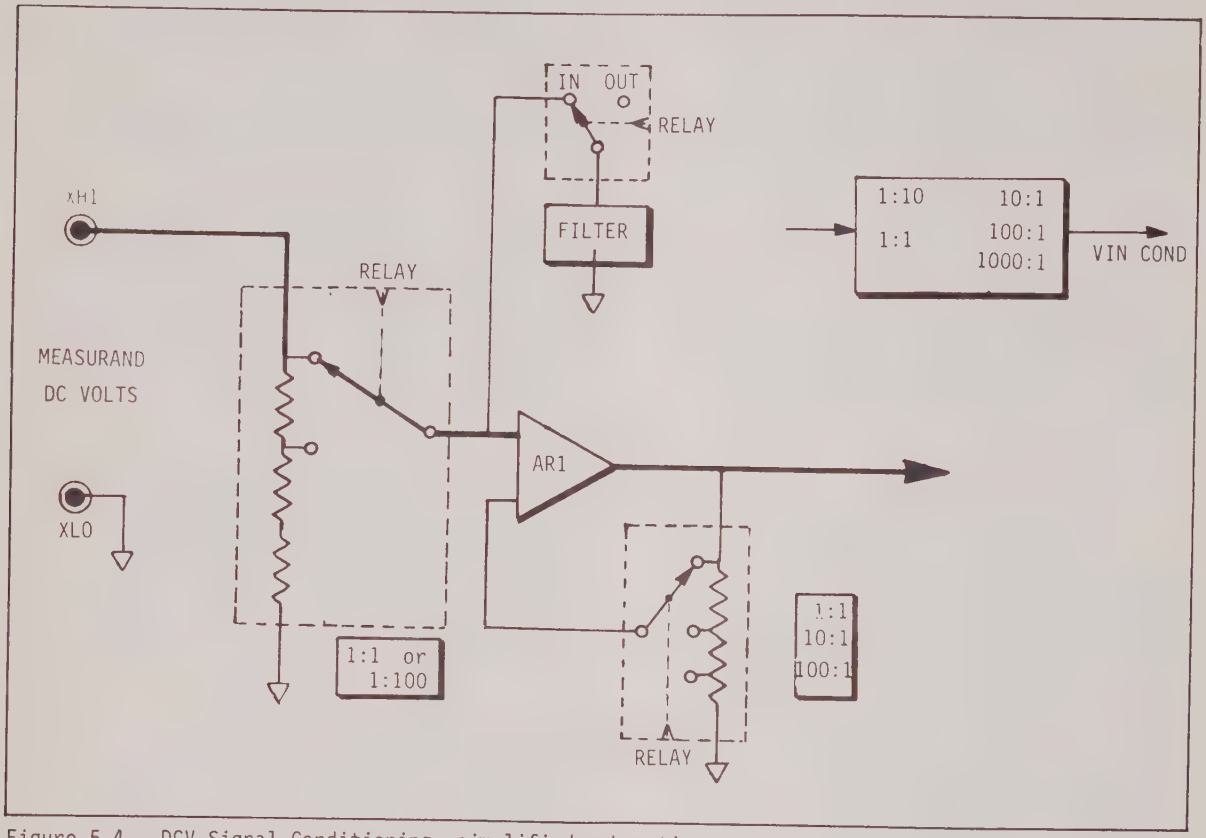

Figure 5-4.. DCV Signal Conditioning, simplified schematic

c. Test inputs are also conditioned and scaled in assembly A5. A 10-volt or 1-volt signal is obtained from the -10 volt reference and scaled through the basic circuit of figure 5-4 so that the displayed result is an overload condition (OVLD) on Range .1; 1.00000 on Range 1; 01.0000 on Range 10; 010.000 on Range 100; and 0010.00 on Range 1K.

5.5.5 A/D Conversion.

a. The conditioned input, VIN COND, and the selected reference, REF, are inputs to the A/D converter Analog Section, Assembly A6. Figure 5-5 is a simplified schematic of this functional unit; the control signals for the phase-controlled switches are generated in the Analog Control, Assembly A7, which are in turn, developed from the master clock, the comparator output, and from the program registers. (Figure 5-5 is a considerably simplified form of the schematic for A6 that is included in Chapter 9.) Control signals transmitted from non-isolated sources in the Program & Status assembly A12, A/D Programming assembly, A8, and Range & Control assembly A13 are converted to isolated signals through appropriate transformer and opto-isolator in Analog Control assembly A7 for use in the A/D Converter assembly A6.

b. The A/D conversion is accomplished in four phases, with suitable pauses as described in paragraph 5.4 for settling of any switching transient effects between phases. The operating elements of the A/D converter are configured for each phase by the actions of symbolic switches A through K (I is not used). The actual switches are configured as series - parallel pairs, but their operating effects are as shown schematically in figure 5-5. We start with Phase 2 because the trigger starts that phase. Auto-zeroing, Phase 1, occurs both between conversions and at the end of a conversion.

c. During Phase 2, switch A is closed, connecting the conditioned input VIN COND as input to 0.5 gain amplifier Z1. Switch D is closed, and the inverted VIN COND is input to

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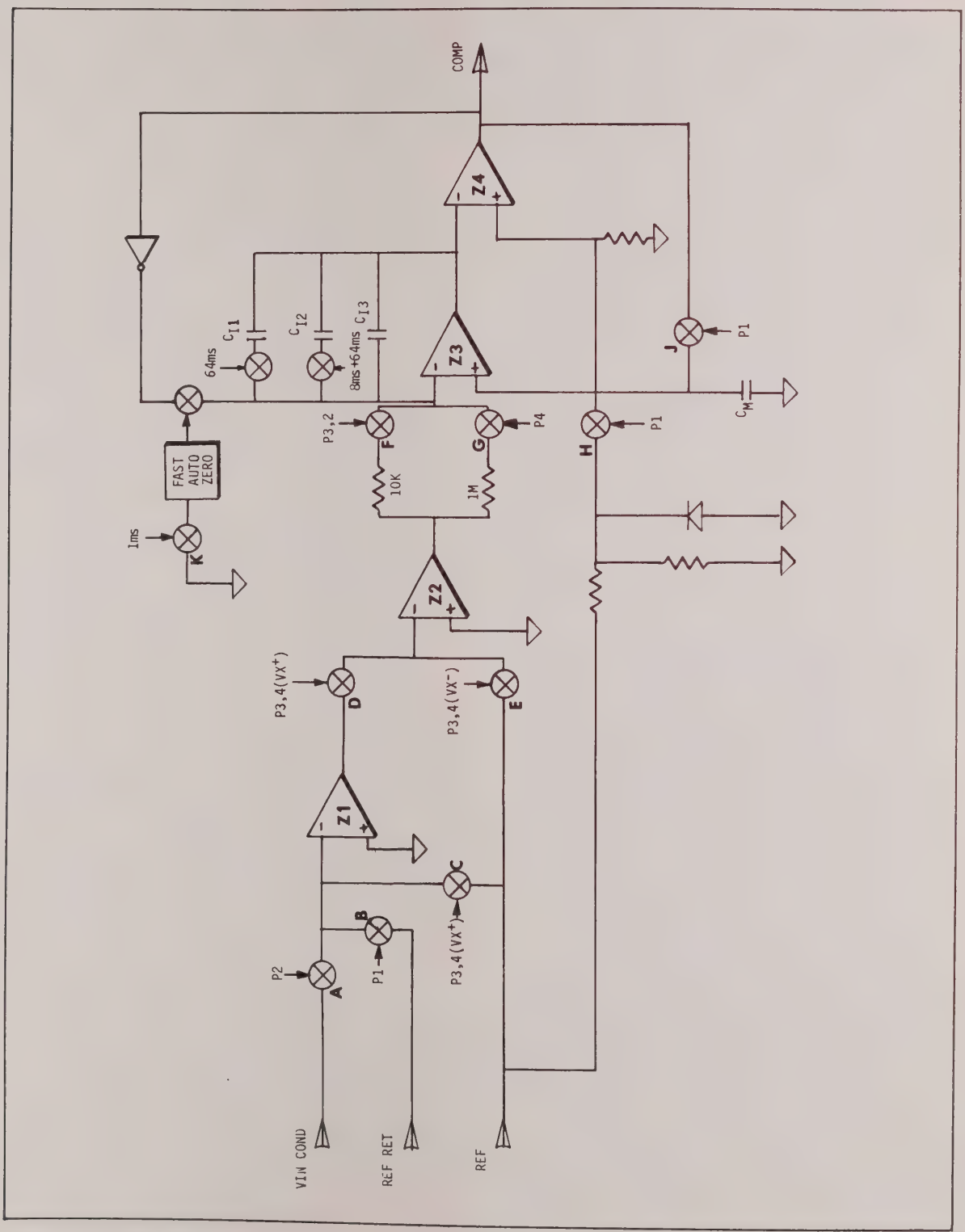

Figure 5-5. Quadraphasic A/D - Simplified Schematic.

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unity gain amplifier Z2, so that the output of Z2 is of the same polarity as the input. The output of Z2 then charges the integrating capacitor in the integrator Z3 via switch F and the 10K resistor. The net charging current is determined by the value of VIN COND and the resistor. The charge stored on the auto-zeroing capacitor, C_M, during the auto-zeroing phase, at the input to Z3 provides an offset correction of very small magnitude. The charging rate time constant is determined by the value of the capacitor C_{I1}, C_{I2}, or C_{I3}, and the resistor 10K which is the charging path during this phase. The capacitor value is relay-selected as determined by the programmed measurement time. As shown in figure 5-5, $C_{I3} \pm 0.027$ uF is in the circuit for a 1 msec measurement time, C_{I3} in parallel with C_{I2} provides a total capacitance of 0.207 for the 8 msec selection, and C_{I1} in parallel with C_{I3} provides a total capacitance of 1.707 uF for 64 msec selection. The integrating capacitor is charged to nearly the same value (about 10V peak for full scale) for a given input signal for any one of the selected integration times: 1 msec, 8 msec, or 64 msec.

d. At the end of Phase 2, the output of comparator stage Z4 is sensed as a polarity signal, transmitted from assembly A6 to Analog Control A7. Assembly A7 includes logic circuitry to compare the polarity of VIN COND with the polarity of the selected reference and develops control signals to connect the A/D configuration for the actual signal and reference polarities for Phases 3 and 4. At the same time, a transformer coupled pulse (POL) is transmitted if the measured value is positive to the Register & Storage assembly A9 to set the polarity in the output data.

e. During the pause at the end of Phase 2, the A/D assembly A6 circuits are set up for the correct polarity reference integration, and analog control assembly A7 circuits determine whether that reference integration should commence with the fast slope, which is opposite in sign to the slope of Phase 2, or whether to change slope to the slow one. This is accomplished by closing switch H, and comparing the integrator output with the .015% threshold at the inputs to Z4. If the fast slope is required, switch F remains closed (figure 5-5), while the capacitor switches remain as programmed by measurement time selection. Switch H remains closed.

f. At the input to A/D, the measurand is disconnected (switch A is opened), and the reference is connected through both Z1 and Z2 stages if of opposite polarity to the measurand (switches C and D close; switch E open). If the reference is of the same polarity as the measurand, the reference bypasses Z1 and is connected first to Z2 (switches C and D open, switch E closed). Since the standard internal reference is -10V, switches C and D are closed for positive measurand inputs when in normal standard measurements.

g. During Phase 3, the comparator Z4 non-inverting input is biased to a value of .015% of range (figure 5-5) while the digitizing counter in Register & Storage A9 begins to accumulate counts at the fast rate (each increment = 100, and full scale count = 100000). The comparator output (COMP) from A6 is continuously monitored in the Analog Control A7 to generate control signals that: (1) switch the integrator from fast to slow rate at the next clock pulse (close G, open F), (2) remove the threshold from Z4 (≠) in A/D assembly A8 (figure 5-5) returning the comparator to its initial state, and (3) signal digitizing counter in A9 to increment at 1/100 of the fast count (control signal SLOPE CHANGE).

h. During Phase 4, when the integration is proceeding at the slow rate (= 1/100 of the fast rate) by switching in 1 megohm in place of the 10 Kohm resistance in the charging current path, the circuitry in Analog Control A7 continues to monitor the comparator output (COMP). When the output COMP changes state again, signifying the end of conversion, the END CONV signal is generated and transmitted to the A/D Programmer, A8, where decision circuits determine the need for range change (if in auto range), or for the display of overload conditions if not in auto or at maximum range. The circuitry of A8 transmits TRANSFER and, if measurand is in-range or if not in AUTO, LATCH signals to the Register & Storage assembly A9. If the count in the digitizing register reaches 200,000 before END CONV is received, then assembly A9 generates an OVERLOAD signal that results in digit blanking on the display assembly A16.

i. Digital output data, in BCD format for each decimal digit is transmitted from the latched register in A9 to the display A16 where BCD-to-7-segment drivers produce the desired data display. Decimal point drivers receive their inputs from the registers in the Range & Control assembly A13, while the polarity sign signal is obtained from assembly A9. Decimal point and polarity sign (if appropriate) are not blanked in overload condition.

j. At the end of Phase 4, at most 2100 counts (COUNTER = 200000) from the start of

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the measurand integration phase, the multimeter is placed in the auto-zero mode of operation. Both the conditioned input, VIN COND, and REF are removed from the input to the A/D by opening switches A and C (figure 5-5). At the same time, switch B is closed and switch J is closed. The former zero's the input to Z1, while the latter closes the loop around the integrator and comparator stages. This configuration drives the remaining charge on the integrating capacitors to zero, and if there are any non-zero offset voltages in the circuit, the zero loop charges capacitor C_M until the integrator Z3 output is equal to the input offset voltage of comparator Z4. The charged C_M introduces the correction for such internal offset voltage in Phases 2, 3, and 4. The autozeroing lasts at least until the counter reaches 240000 and continues until conversion starts.

k. When in auto-zero and the measurement time is 1 msec, there would not have been sufficient time in the remaining counts to completely discharge the integrating capacitors without additional circuits. Therefore, the A/D conversion assembly A6 generates a switch control signal that introduces a fast auto-zero circuit at the input to stage Z3 to assure complete discharge before auto-zeroing is completed. Note: At measurement time = 1 msec, a minimum of 104 usec may remain for autozeroing.

5.5.6 Auto-Ranging.

a. If in auto-ranging, and the digitized value exceeds 199999, then the A/D Programmer A8 initiates an auto-ranging delay and generates a MAX RANGE command, if not already at High Range, to Range & Control A13. It also prevents the latching operation, keeping the display from receiving a result until after the ranging operation is completed.

b. In auto-ranging, Register & Storage A9 determines whether a down ranging action will be effective. If not already at low range, and if the two leading digits transferred to the shift register at END CONV are both zero, then A9 generates and transmits the down range enable control, DR ENABLE, to the Programmer A8. Receipt of this control signal causes A8 to initiate the auto-ranging delay and to generate a pair of SHIFT and MODE control signals for transmission to the Register & Storage A9. There, these signals cause the register values to shift up one decade, while also shifting the range counter and the decimal point down one decade range. Under clock control in A8, the process is repeated until leading zero's are eliminated, or until low range is reached.

5.6 OPTIONS

5.6.1 Measurand Signal Conditioning.

a. When ac voltage signal conditioning option is installed, the connected measurand (XHI and XLO) is switched from the DC Signal Conditioner, A5, to the AC Signal Conditioner, A4, and back. In A4, the input is scaled, rectified, and filtered, so that the conditioned dc output of A4 (COND AC) may be further scaled by A5 to become the dc input (VIN COND) to A/D converter, A6. Relay control signals, connected from A13 via optoisolators on A7, determine the scaling factors for the ac measurand. Displayed data may be either sensed average value of the full-wave rectified ac input scaled for the rms of an equivalent sine wave, or true rms of the input, depending upon the ACV option installed.

b. When Kilohms Signal Conditioning option is installed, option assembly A2 generates a driving current, scaled in magnitude for the selected range, to be connected from R_X (HI and LO) to the unknown resistance. The resultant dc voltage across the unknown resistance becomes the measurand to be connected as XHI and XLO) and thence to DC Signal Conditioner assembly A5. When in resistance measurement function, RANGE 10K is effective, and in-range measurements up to 19,999.9 kilohms are possible.

5.6.2 Reference Signal Conditioning.

a. When Ref AC Signal Conditioning option is installed, permitting ratio measurements with respect to an externally connected ac signal, the external reference is connected as REF HI and REF LO to installed assembly A3. There the signal is rectified, filtered, and partly scaled so that additional scaling in assembly A5 results in the dc input (REF) to A6.

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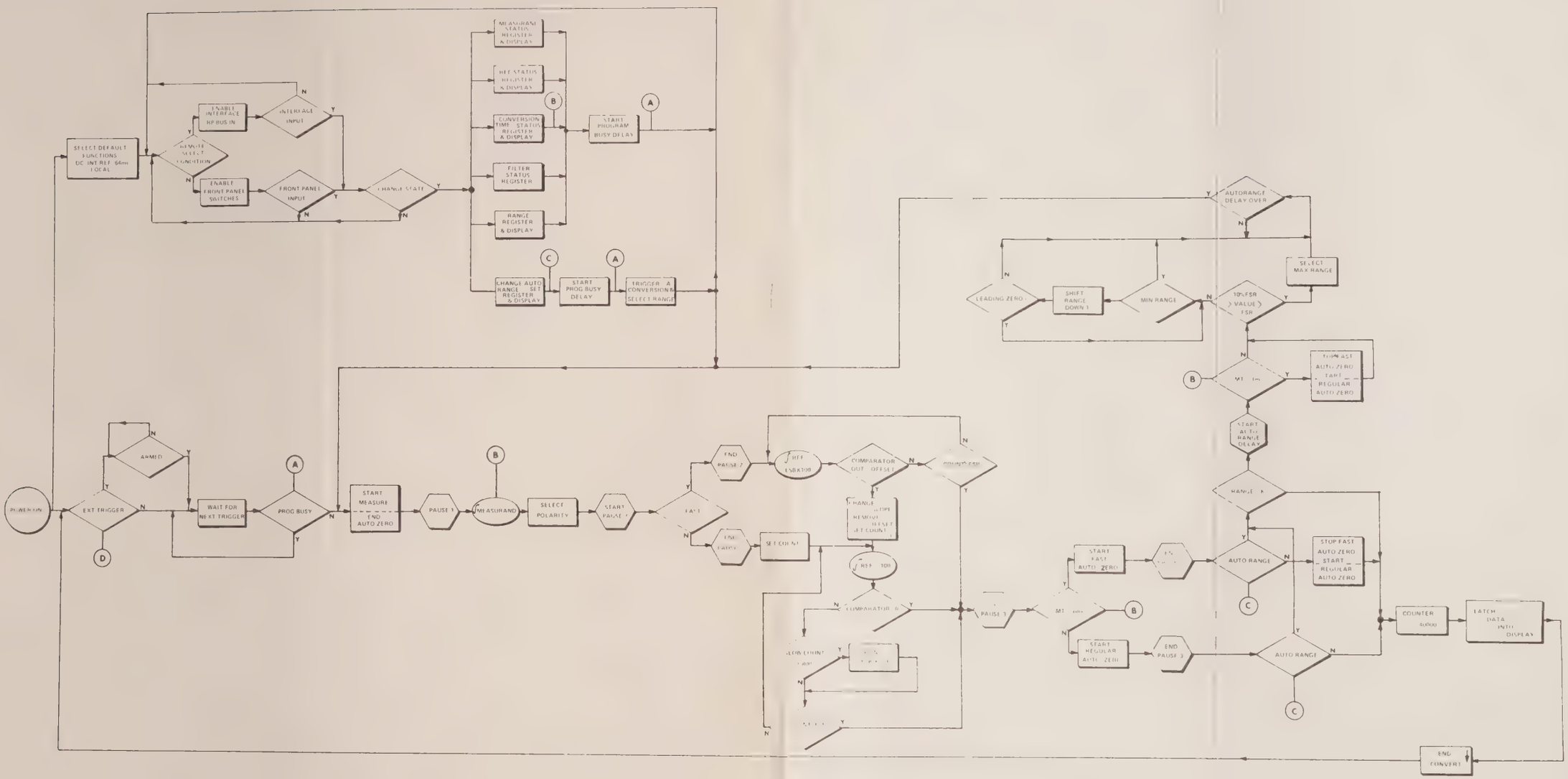

Figure 5-1. Logic Flow Block Diagram

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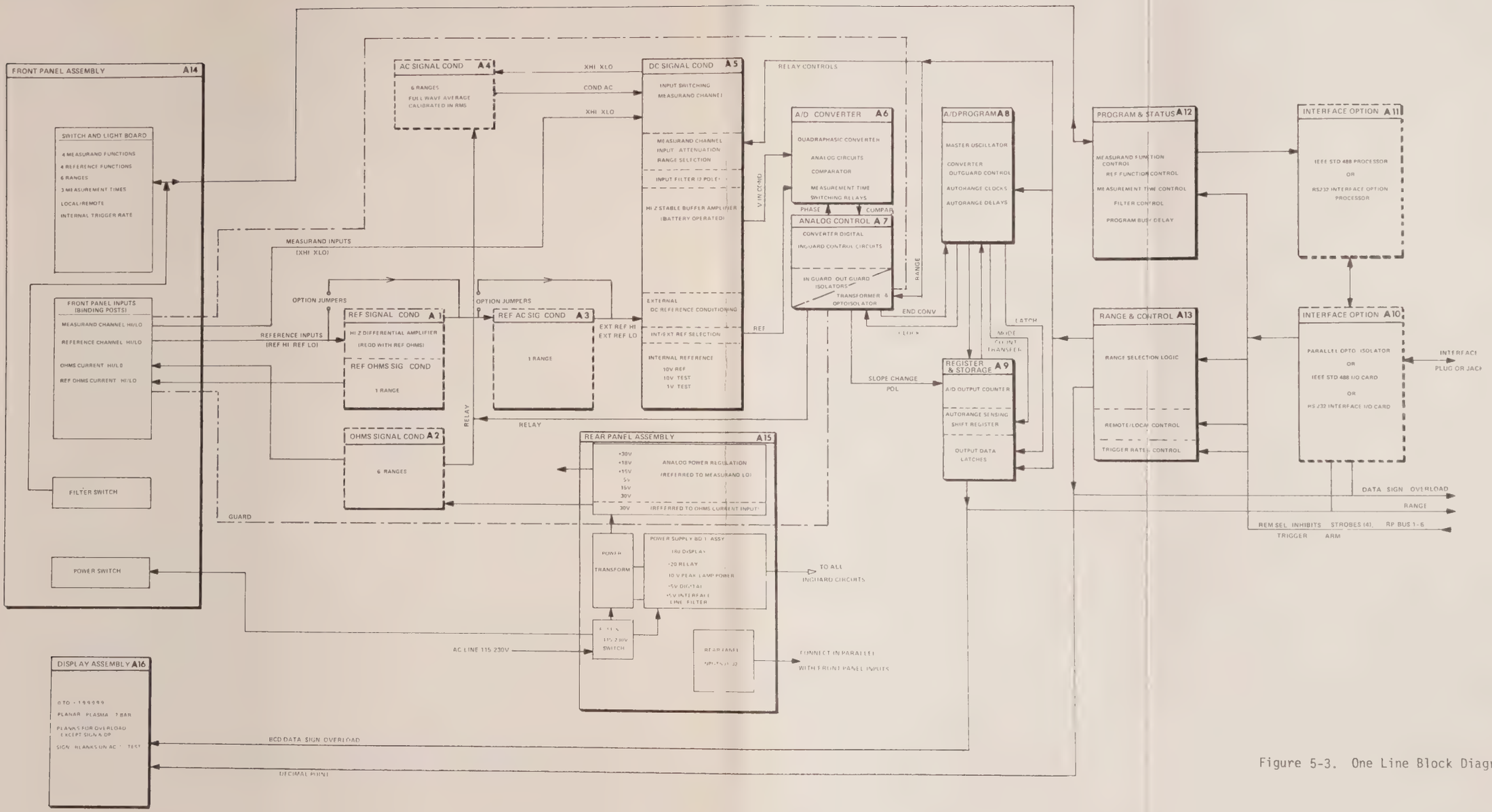

Figure 5-3. One Line Block Diagram

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6
MODULE OPERATION

6.1 GENERAL

a. This chapter describes the operation of each replaceable module assembly as an independent unit. Refer to Chapter 5 for the interaction of these modules, and to the schematics in the back of the manual for detailed circuitry. Some of the circuit descriptions in this chapter refer to simplified schematics incorporated in the text. These are derived from those in the back of the book and are used for illustrative purposes only; the reference schematics in the rear of the book should be referenced for complete detail.

b. Table 6.1-1 identifies the Data Precision drawing numbers for the assembly, schematic, and parts list of each module. Only those modules needed for the ordered configuration are incorporated in each Model 7500. However, chapter 6 includes a circuit description of the optional signal conditioning modules for AC Signal Conditioning (A4), Ohms Current Source (A2), Ref AC Signal Conditioning (A3), and Ref Ohms (A1), whether or not included in the ordering information. The chapter includes the circuit description of only the interface modules (A10 and A11) delivered with the ordered Model 7500. Refer to chapter 1 for ordering information.

c. The sequence of module descriptions in this chapter considers first those modules comprising the Basic configuration, followed by the measurand and reference options, and concluding with the appropriate interface options. Thus:

6.2 DC Signal Conditioning (A5)
6.3 A/D Converter (A6)
6.4 Analog Control (A7)
6.5 A/D Programming (A8)
6.6 Register & Storage (A9)
6.7 Range & Control (A13)
6.8 Display (A16)
6.9 Program & Status (A12)
6.10 Power Supplies and other Rear Panel (A15)
6.11 Front Panel (A14)
6.12 AC Signal Conditioning (A4)*
6.13 Ohms Current Source (A2)*
6.14 Ref AC Signal Conditioning (A3)*
6.15 Ref Ohms (A1)**
6.16 Interface (A10)**
6.17 Interface (A11)**

* Options
** As ordered for specific interface

6.2 DC SIGNAL CONDITIONING (A5)

6.2.1 General.

Module A5 conditions DC input voltages by scaling the input amplitude so that 20 volts produces a counter total of 200,000 in the reference integration phase. This module also performs the following functions:

a. It provides standard test voltages of -10V and -1V dc as measurands for the TEST mode operating function.

b. It conditions an external dc voltage or the dc output of another optional conditioner to be used as a reference for ratio measurement when any external reference mode of operation is programmed.

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TABLE 6.1-1 DM7500

ASSY REF	ASSY TITLE	SCHEMATIC DWG. NO.	ASSY DWG. NO.	PARTS LIST NO.
A1	Ref Ohms Conditioning	55-1029	57-1029	50-1029**
A2	Ohms Current Source	55-1010	57-1010	50-1010
A3	Ref AC Sig Conditioning	55-1028	57-1028	50-1028*
A4	AC Sig Conditioning	55-1009	57-1009	50-1009
A5	DC Sig Conditioning	55-1008	57-1008	50-1008Ŧ
A6	A/D Converter Analog	55-1000	57-1000	50-1000
A7	Analog Control	55-1002	57-1002	50-1002
A8	Prog. A/D	55-1004	57-1004	50-1004
A9	Reg. & Stor.	55-1003	57-1003	50-1003
A10	Interface	As installed***		
A11	Interface			
A12	Prog. & Status	55-1006	57-1006	50-1006
A13	Range	55-1007	57-1007	50-1007
A14	Front Panel	55-1015	57-1015	50-1015
			57-1018	50-1018
A15	Power Sup. & Rear Panel	55-1012	57-1012	50-1012
		55-1013	57-1013	50-1013
			57-1027	50-1027
A16	Display	55-1001	57-1001	50-1001
A17	Extender Card		57-1025	50-1025

Ŧ Amp. Sub Assy 50-1032, 1031

* Ref AC Options
01 0.1 50-1033
02 1V 50-1034
03 10V 50-1035
04 100V 50-1036

** Ref Ohms Options
02 1K FS 50-1037
03 10K FS 50-1038
04 100K FS 50-1039
05 1 MEG FS 50-1040
06 10 MEG FS 50-1041

*** Interface Option
01 – Parallel Opto-isolated, Open Collector Out.
02 – Parallel Opto-isolated, 2.2K Pull Up, LPTTL in
10 – IEEE Standard 488 GPIB Microcomputer Controlled
30 – RS-232C/TTY Interface, Microcomputer

TABLE 6.2-1

DCV Scaling & Range Determination

Range Control			Relay			Gain Factors			Range
A	B	C	K2	K5	K4	Input to AR1	Output of AR1	NET	
1	0	0	0	0	1	1:100	1:1	1:100	1000V
0	1	0	0	1	0	1:100	10:1	1:10	100V
1	0	1	1	0	1	1:1	1:1	1:1	10V
0	1	1	1	1	0	1:1	10:1	10:1	1V
1	1	1	1	1	1	1:1	100:1	100:1	0.1V

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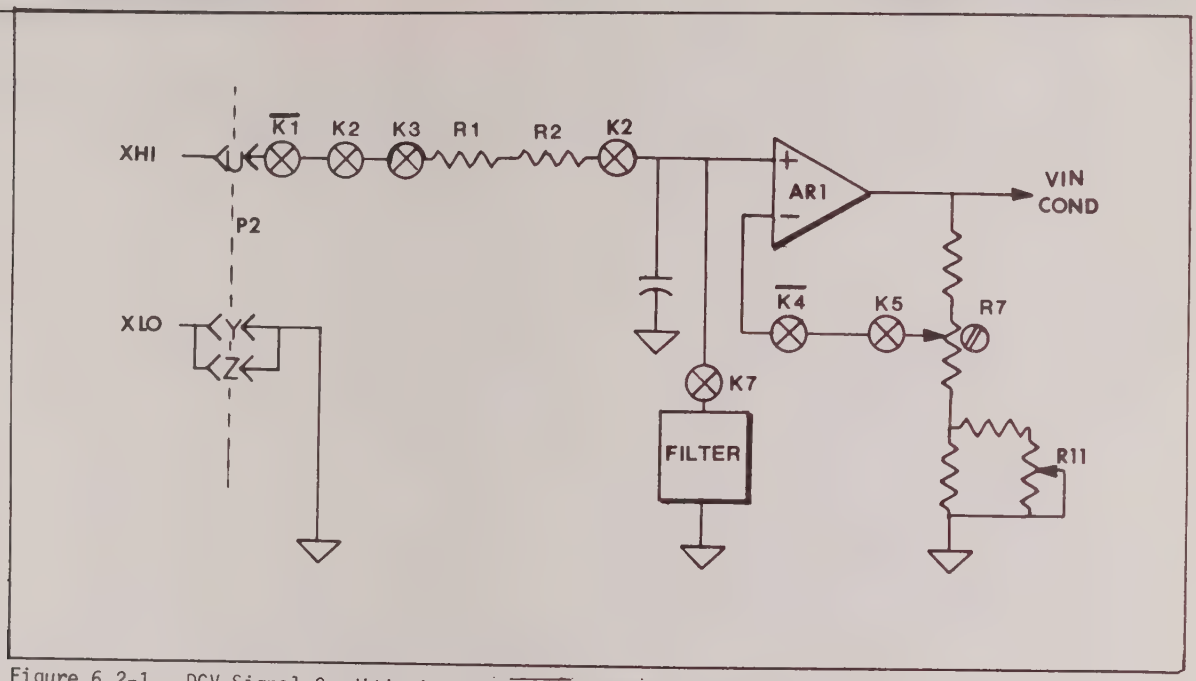

Figure 6.2-1. DCV Signal Conditioning for $\overline{\text{RANGE}}$ A·RANGE B·Range C

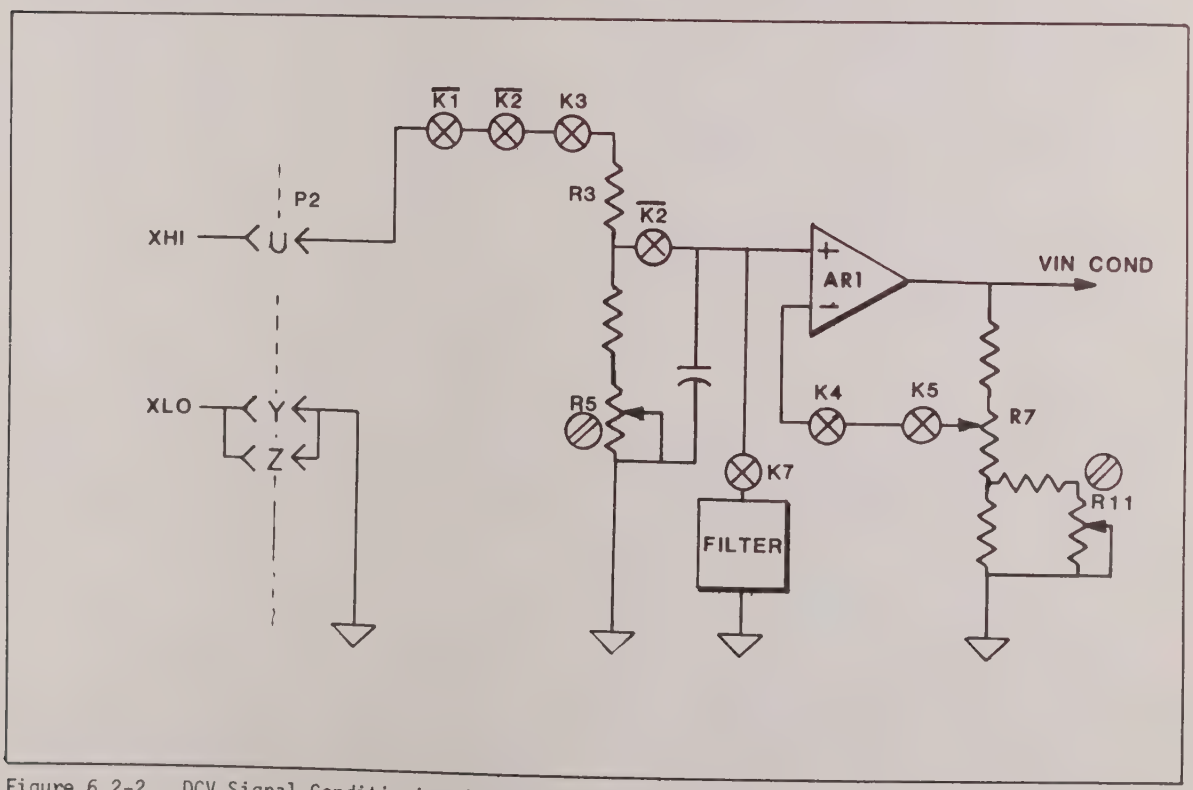

Figure 6.2-2. DCV Signal Conditioning for RANGE A·RANGE B·$\overline{\text{RANGE C}}$

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c. It conditions the dc outputs of ac and kilohm measurands and ref ac, dc and kilohm signal conditioners when those options are installed, and the appropriate operating function is selected.

d. It senses the polarity of the reference for use in displaying the polarity whenever applicable and to control the selection of reference integration.

Drawing 55-1008 is a complete schematic of the DC Signal Conditioning circuitry, and it is reproduced in chapter 9.

6.2.2 Range-Controlled Relay Action.

a. Module A5 is the signal conditioner for all inputs to the A/D converter, and it is configured to introduce the needed attenuation/amplification factors by the operation of measuring function and range selection relays. The input to Module A5 may be scaled in a combination of the following:

(a) Attenuation by resistor divider R3, R4, and R5 at the input to AR1

(b) Direct connection to AR1 via protective resistors R1 and R2 (may be considered a special case of [a] above.)

(c) Selected gain by the resistor divider R6-R11 in the feedback path around AR1.

b. The six possible ranges are indicated by the levels on three lines RANGE A, RANGE B, and RANGE C, in combination (only 6 of the 8 possible combinations are used). In DCV measuring function, the highest range, RANGE 10K, is never actuated.

c. When in DCV mode, XDC is high, enabling the operation of range relays K2, K5, and K4 through transistors Q1, Q2, and Q3, respectively. In addition, since XAC is low, Q4 is not on, and LOW RANGE signal has no effect on DCV measurements. Table 6.2-1 summarizes the action of the circuitry in setting up the attenuation factors for the effective combinations of RANGE A, B, and C levels. For example, per Table 6.2-1, low, high, and low levels of A, B, and C, respectively result in a net attenuation of 1:10 on input signals connected between terminals A5P1-U and A5P1-Y,Z. Since 10 volts at the input of AR1 results in a 100,000 count, an input to XHI of 10 x 10 = 100 volts will produce the same count and digit display. Automatic positioning of the decimal point provides for scaling of the reading. Figures 6.2-1 and 6.2-2 illustrate the circuit configurations when in DCV mode and RANGE A, B, and C are low, high, high (Figure 6.2-1) and high, high, low (Figure 6.2-2).

6.2.3 Filter.

When in DCV or Kilohms mode, relay K7 may be operated to insert an active filter containing amplifier Z6 at the input to AR1. The 2-pole low-pass filter attenuates 60-Hz components of the dc measurand by 43 db (nominal). The 3 db point is 5 Hz, and attenuation rises 40 db per decade of frequency.

6.2.4 Quadrant.

The output (QUADRANT) of comparator amplifier Z3 is clamped through limiting resistor R33 and circuits in Analog Control assembly to either ground or -5V. It will be high if either the internally supplied -10V reference is connected or if the sign of the externally connected reference is positive. The level of the QUADRANT output of Module A5 at A5P1-N is used to determine the polarity of the displayed data, when applicable, and to control the reference switching of the A/D converter, A6.

6.2.5 Reference and Internal Test.

a. A precision reference of -10V is developed in the circuit containing amplifier Z2, thermally stabilized reference diode VR1 and feedback divider network R21 - R26. A tap on the divider and adjustment network R28 - R31 provide a precise -1V signal for test use.

b. In INT REF operation, the internal precision -10V reference is used as the integrand during the reference integration, phases 3 and 4, of the A/D conversion. The reference value of -10V may be calibrated by potentiometer R23, in the feedback path of Z2.

c. In test operation, TEST control signal is a high level at connector A5P2-7, operating relay K3 and enabling the operation of relays K2, K5, and K4, as for normal DCV measurement. Relay K3 operation places a precision -1V signal as a possible direct input to AR1, and also places a precision -10V signal as a possible attenuated input to AR1. The range selection determines which of these inputs is conditioned for input to the A/D module.

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d. The relay-selected conditioned input for the selected range scales in TEST and in INT REF mode are shown in Table 6.2-2. Operation of RANGE 10K pushbutton results in selection of RANGE 1K.

TABLE 6.2-2

Display Values for INT TEST

RANGE	TEST SIGNAL	CONDITIONED TEST INPUT TO A/D	NOMINAL DISPLAY
1K	-10V	-0.1V	0010.00
100	-10V	-1V	010.000
10	-1V	-1V	01.0000
1	-1V	-10V	1.00000
0.1	-1V	-23V	Overload

6.2.6 External Reference.

In all ratio measurements, the externally supplied reference is converted to a dc voltage between ±1V and ±11V by optional conditioners (if installed), and then the dc voltage is also conditioned in Module A5. The external DC voltage is applied to the input of a differential amplifier circuit including Z1; its gain may be adjusted by potentiometer R13 which adjusts the ratio of feedback divider R12, R13, and R14. The common mode rejection may be improved by adjusting the balance of the impedances of the input legs to Z1 by potentiometer R16, in the low side of the input leg. The zero offset of Z1 is adjusted by potentiometer R18.

6.2.7 AC Signal Conditioning.

Module A5 is also used in the conditioning of AC voltage measurands. In AC Amplifier AR1 operates as a unity gain buffer on all except the 0.1V Range where it operates at a gain of 10. Its action in this mode is further described when explaining the operation of the ACV signal conditioning. Note that when in ACV mode, XAC is high, operating relay K1, which places the AC Signal Conditioner in the path from XHI to Cond AC.

6.2.8 Kohms Signal Conditioning.

In the KΩ mode, Module A5 provides the voltage sensing function, while Module A2 provides a standard current to the resistance. Amplifier AR1 operates at a gain of 10 on all ranges except the 0.1K range, when it has a gain of 100. The operation of Module A5 when used in the K Mode is described in paragraph 6.13. Note that XΩ control is high when in KΩ Mode, so that K4 and K5 are operated when LOW RANGE is high during this mode.

6.3 ANALOG A/D (A6)

6.3.1 General.

a. Module A6 receives the conditioned measurand input from Module A5 and the conditioned internal or external reference. Under program control signals transmitted by Analog Control Module A7, Module A6 develops output signals from its comparator circuit (Z4) to be used in (1) determining the polarity of the measurand, and (2) determining the interval needed in the reference-integration phases to balance the measurand-integration for in-range inputs (see chapter 5). The detailed schematic is shown in Data Precision drawing 55-1000 included in chapter 9.

b. As shown in the schematic, the very high speed switching actions required to connect and disconnect measurand, positive reference, negative reference, and integration time-constant elements are accomplished by shunt-series pairs of FET solid-state switches. Relay circuitry is used to configure the A/D converter corresponding to selection of conversion times of 1, 8, or 64 m sec. The shunt FET switches for each switching action provide a clamp on the input side of each switch so that when the switch is "open," the input will not inadvertently close the switch by applying a high signal of proper polarity. The shunt switch also minimizes leakage and reduces capacitively-coupled transients. In less critical locations the shunt FET is connected only as a leakage diode clamp.

c. The A/D Converter essentially contains an input section of two stages, an integrator section with switch-selected integration time constants, a comparator section, a group of clamp limiting stages, and relay control circuitry.

6.3.2 Input Stages.

a. Buffer amplifiers Z1 and Z2 are connected in series during the measurand-integration phase (Phase 2), and the double inversion maintains the input polarity at the input to the integrator stage Z3. The combined gain through the two stages is 1/2, resulting from the divide-by-two action of the feedback circuit around Z1 and the unity gain around Z2 (when in Phase 2).

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b. When in Phases 3 and 4 (reference integration), a negative reference is connected through Q7 for positive measurand inputs, and the input stages are configured in the same arrangement as for Phase 2. If the measurand is negative, then the negative reference by-passes Z1 (Q7 opens), and is connected to Z2 through Q11. In this instance, the feedback and input network around Z2 introduces a divide-by-two action so that the input to the integrator stage Z3 is of opposite polarity to that of the measurand (only one inversion instead of two) and of the proper amplitude.

c. When in Phase 1, Auto-zero, the input to Z1 is connected to REF RET which is the multimeter's analog reference point by switch Q4, while all measurand and reference inputs are removed.

d. Stages containing active elements Z5 and Z6 are configured into clamp circuits that are active in Ratio Mode of operation. If ratio limits are exceeded, then diode Q21 or Q22 conducts, limiting the signal to integrator stage Z3. The two sections of Z5 form an absolute value circuit; the output is equal in magnitude to the actual conditioned reference but always of negative polarity. The two sections of Z6 compare the outputs of Z1 and Z2 to the reference magnitude and actuate the clamps Q21, Q22 if the maximum numerator signal exceeds twice the reference (denominator) signal.

6.3.3 Integrator.

a. The integrating capacitance is determined by the combined actions of relay K1 and K2, while the time constant change from Phase 3 to Phase 4 is determined by the action of series-shunt FET switches Q14, Q15 and Q16, Q17 in switching the resistor in the RC charging-discharging path. Relay action depends upon the selection of the conversion time of 1ms, 8ms, or 64ms, and the operation is summarized in Table 6.3-1. Note, in Drawing 55-1000, that relay control signals, IMP, are optically isolated. The 1:8:64 ratios in capacitance (within the component tolerances) are designed so that the integrating capacitor will be charged to the same voltage value for a given measurand, regardless of the selected measurand integration time.

b. During Phase 1 Auto-Zero, when the input to Z1 is shorted to reference return, a feedback loop around Z3 and Z4 is closed by Q19, and the operation of that closed loop charges capacitor C20 (at the non-inverting terminal of Z3) to equal the non-zero value appearing at the inverting input terminal to Z3. This action corrects for all slow offset voltage drifts in stages Z1, Z2, Z3, and Z4. The auto-zero circuits also provide for rapidly reducing the charge on the integrating capacitance which may remain at the end of an out-of-range conversion cycle. Flip-flop Z8 is connected as a one-shot that is triggered by EOC when 1ms measurement time has been selected (= 8ms - 64ms). The triggered Z8 momentarily places a high level on its $\overline{Q}$ output and a low level on the Q output. In the one-shot interval, these levels open gate Q24 and close Q23 creating an additional feedback loop that rapidly discharges the integrator capacitor after an out-of-range conversion.

6.3.4 Comparator.

a. The comparator stage, with active element Z4, is used in the following conversion functions:

(1) At the end of Phase 2 (measurand integration) its output polarity is indicative of the measurand polarity. Since the conditioned measurand ($V_{IN\ COND}$) goes through 4 inverting stages, the output at A5P2-3 is of the same polarity as the input.

(2) During the pause before the start of the reference integration (Phases 3 and 4), the circuit compares the voltage on

Table 6.3-1

Conversion Time Selection	Relay Operation	Net Nominal Integrator Capacitance
1msec	None	.027 uf
8msec	K2	.180 + .027 = .207
64msec	K1	.027 + .180 + 1.500 = 1.707

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the integrating capacitor with a calibrated non-zero offset voltage proportional to the reference. If the voltage is greater than the offser, then the fast slope discharge path is used for Reference integration Phase 3. If not, then the comparator output causes the slope to be switched and the offset to be removed, and the reference integration starts with Phase 4.

(3) During Phase 3 (fast Reference Integration) the circuit continues to compare the voltage on the integrator capacitor with the offset. When the COMPARATOR signal changes polarity, it causes the slope to be changed and the offset to be removed, to start Phase 4. This action returns the output of the comparator to its original polarity.

(4) The next change in COMPARATOR output polarity during Phase 4 occurs when the integrator output voltage passes the zero point and initiates the end of conversion of an in-range measurand value.

b. Switch Q20 controls the application of an offset voltage derived from the reference. The switch is on during Phase 3. The offset corresponds to a count of about 300 and is applied to the non-inverting input of Z4 when Q20 is closed. When the switch is opened, the comparator reference is essentially zero.

c. Switch Q19 closes the auto-zeroing servo loop to include Z3 and Z4.

d. Z4 is a high-gain comparator amplifier. Its input is clamped by CR2 and CR3 to prevent input voltages in excess of its ratings. Current limiting network (Q18, CR1, R58, %27) prevents overload of integrator Z3 when CR2 or CR3 conduct.

e. Network R31, R33, R32 provides a 4-count nominal offset at the input to Z4. This offset guarantees that Phase 4 will have a minimum duration in excess of the digital delay in processing the comparator output. The 4 excess counts are removed digitally by counter elements in Module A9, and the proper combination of offset and delay is obtained by R33 to develop a zero reading for a zero input.

6.4 ANALOG CONTROL (A7)

6.4.1 General.

The Analog Control Module A7 performs the following functions:

(a) Develop isolated control signals to program the Signal Conditioning and Converter Modules. The isolation is accomplished in Module A7 by transformer coupling for control signals that operate on transitions, and by opto-isolators for control signald operating on levels.

(b) Isolate the train of clock pulses for use within the module.

(c) Establish necessary timing relationships among the related switching control signals to assure properly phased operation for the necessary switched operations of Module A6.

Note that the digital circuits in this Module (A7) are operated from the isolated analog power supply section ground and -5V. Therefore, logic "zero" level is -5V and logic "one" is ground (if common mode voltage at Vx is zero).

6.4.2 Timing Control.

a. The flip-flops that generate W, X, Y, and Z control levels in Z7-2, Z7-5, Z11-9 and Z9-9 control the fixed timing portion of the A/D conversion process. The sequence is started by START CONV A at A7P1-P, setting W high (TP4), and it is advanced by pulses on PROG (A7P1-12): at the end of each pause, the end of Measurand integration, and the counter value of 240000 (end of conversion cycle). The variable timing portion of the A/D conversion process is controlled by Z11-5, Z1-5, and Z9-5 in response to COMPARATOR input at A7P2-A and CLOCK pulses, input at A7P1-14.

b. Fast integration is controlled by Z1-8 , whose transitions are clock synchronized. Q1 and Q2 drive the control signals to ground level in minimum rise time counteracting any effects of capacitive loading on these circuit paths. During the reference integration phase (or Pause #2 if below the switch-over threshold at the comparator) presetting Z1-4 (signal SL in the schematic) indicates that the slope should change from fast to slow integration at the next clock pulse. Presetting of Z9-4 indicates that the comparator has passed through zero; that slow reference integration is complete; and that data transfers should occur in the non-isolated digital circuits.

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6.4.3 Opto-Isolated Control Levels.

Signals controlling selection of conversion time (1ms, 8ms, and 64ms), filter, and range (A, B, and C) are optically isolated by Z13 and Z12.

6.4.4 Polarity.

a. The sensed measurand polarity is generated at the output of Z11-5 and transformer coupled to the digital display circuitry through connector A7P1-13 as signal POL. The D input to Z11-2 is determined by the relative polarities of COMPARATOR and QUADRANT, and this polarity is transferred through Z11 at the end of Phase 2 by the action of Z7-6, under program control. QUADRANT is high if the reference polarity is INT REF or if a positive EXT DC REF is used. It is low if a negative EXT DC REF is used. At the end of Phase 2 (Measurand integration) COMPARATOR is the same polarity as the Measurand. Thus, when inverted COMPARATOR at Z4-6 is "Exclusive OR gated" with QUADRANT, the output of Z10-6 is high, causing a + (plus) polarity selection when MEASURAND and QUADRANT are of same polarity, and a - (negative) polarity selection if of opposite polarity. Polarity information is stored in FF Z11-5 for use in Reference Integration. All measurands will be displayed with correct polarity, when applicable, including RATIO measurements. Polarity information at Z11-5 also controls the switching of amplifier stages in Module A6 so that the appropriate reference polarity is used during Reference Integration.

6.4.5 Timing Waveforms.

The timing relationships among the A/D transformer-coupled control signals are included in the waveform diagrams of Figure 6.4-1.

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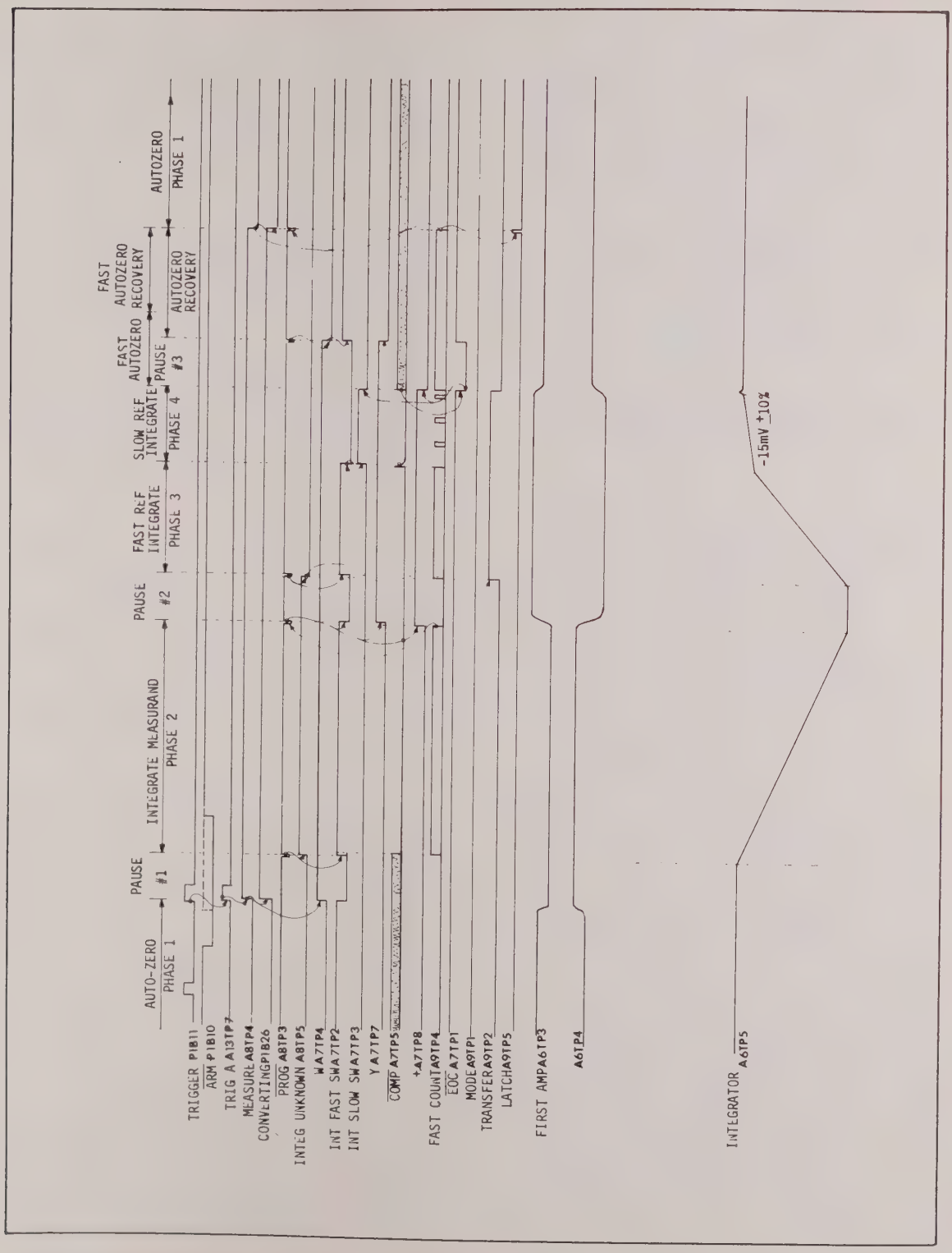

Figure 6.4-1. Timing Waveforms - Positive In-Range measurand

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6.5 PROGRAMMING A/D (A8)

6.5.1 General.

The Programming A/D module performs the fixed sequence digital logic functions that control the quadriphasic operation of the A/D converter. These include:

(a) Dividing the master oscillator frequency into scaled counter and clock pulses;

(b) Decoding the register count value at end of conversion and generating appropriate autoranging control signals;

(c) Generating the basic program control signals for the A/D converter, incorporating the designed pause intervals.

6.5.2 Pause Timer & Clock Rate Divider.

a. The basic oscillator rate of 3.84384 MHz, generated by a feedback loop through crystal resonator Y1, is divided by four and eight in Z7 to generate nominal 1 MHz and 500 KHz signals at A8P1-P and -8, respectively.

b. When conditions for initiating a conversion have been met (TRIG A high or AUTO $\overline{\text{RANGE DELAY}}$ completed if applicable, and $\overline{\text{PROG BUSY}}$ high), the measure flip flop Z11-3 generates a control level to gate the oscillator into the divider chain Z3, Z5, and Z6. The divider performs two functions:

(1) It establishes the durati n of each pause by counting from zero until the carry into Pause End FF (Z6-5) 64 oscillator cycles (16.65msec) later.

(2) During Phase 2, Phase 3, and Phase 4 integration intervals, it develops the slower clock rates required by the selection of either 8ms or 64ms conversion times.

c. The timing intervals from the divider chain are gated by the selected conversion time such that 3400 resulting count intervals last for the duration of the selected conversion time (1, 8, or 64msec), and exactly 1000 clock intervals define the measurand integration interval. The measurand integration time is designed to be exactly one cycle of 60Hz (or 50Hz for Model 7500E) for the 64ms conversion time in order to optimize normal mode noise rejection at line frequency.

d. The $\overline{\text{COUNT}}$ pulse train, at A8P1-4, is gated by the $\overline{\text{PAUSE}}$ control signal in Z8-3 so that the accumulating counter will not receive COUNT pulses during the programmed pauses. The period of each count pulse is about 0.26msec, 2msec, or 16.6msec, determined by the selected conversion time.

6.5.3 Program Cycle.

a. The timing waveform, $\overline{\text{PROG}}$, at A8P1-R introduces negative pulses for one CLOCK pulse interval, as gated through Z9-6, at the end of each pause and at the end of the measurand integration phase while Z8-4 adds another pulse at the end of a full conversion cycle. The total conversion cycle is limited to counter output of 240,000 through the action of Z11-3 which is cleared, and by Z13-6 which is set by the appearance of high levels from the counter silumtaneously at A8P1-U (40,000 counts) and A8P1-T (200,000 counts). $\overline{\text{PROG}}$ (TP3) advances the state of the Analog Control Module A7 from phase to phase.

b. Flip-flop Z6-5 is set the duration of Phase 2, measurand integration and the second pause. When the counter accumulates 1000 counts (each of X100 equivalent display value), the 1×10^5 input at A8P1-H goes high. The signal, through gates Z9-3, Z9-8, and Z9-6 starts the second pause at Z11-9. At the end of the second pause, the output at Z11-6 clocks Z6 to signal the end of Phase 2 as a flag for external programming devices that measurand integration is complete.

c. The end of the second pause advances the program, initiating the reference integration Phase 3 by clocking Z13 at Z13-9. This, in turn, removes the register reset signal that was active during the second pause when it cleared the count to zero.

d. The end of Phase 4 is signalled either by the appearance of a high level at A8P1-13 (END CONV) during the measure cycle, or by the counter reaching 240,000 (high levels A8P1-T, and on A8P1-U).

6.5.4 Register & Storage Control.

a. Module A8 also generates the signals that control the accumulation of COUNTS in the Register and Storage Module. The LATCH signal (A8P1-15) is high (latching the new value in the output registers) when the counter reaches 240,000 (see gate Z14-6) and there is no autorange delay.

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b. A TRANSFER control signal at A8P1-7 is generated either on receiving END CONV from Analog Control (A7) for an in-range signal (via Z16-8, Z14-8, and Z15-5) or when the counter reaches 200,000 (from Z4-6) if overloaded.

c. A SHIFT control signal at A8P1-8 is generated during an auto-range delay. This, in conjunction with a MODE signal at A8P1-V that is generated when down ranging in auto-ranging mode, shifts the value in the storage register in 4-bit BO groups (in Module A9) until an appropriate range is selected, by detecting the presence of a non-zero BCD digit in the register.

d. The $\overline{\text{MAX RANGE}}$ signal at A8P1-Y is a command at A8P1-6 (active low) to the Range Module to go to the maximum range when in auto-ranging mode and when $\overline{\text{HIGH RANGE}}$ indicates it is not already on that range.

e. The AUTO RANGE DELAY interval is determined by the status of the filter in the DCV measuring function; it is shortened to 40msec when no filter is used, and is 350msec in all other circumstances. The delay instrumentation is accomplished by the circuitry including delay-flop Z17.

f. During the autorange delay interval, the new range is selected, autozero recovery occurs, and analog settling on the new range is conpleted. CONVERTING is held active, and LATCH is suppressed during the delay. The end of AUTO RANGE DELAY triggers a new conversion via C3 and Z8-10.

6.5.5 Timing Waveforms.

Figure 6.4-1 and Figure 6.5-1 include some of the waveforms developed in Module A8.

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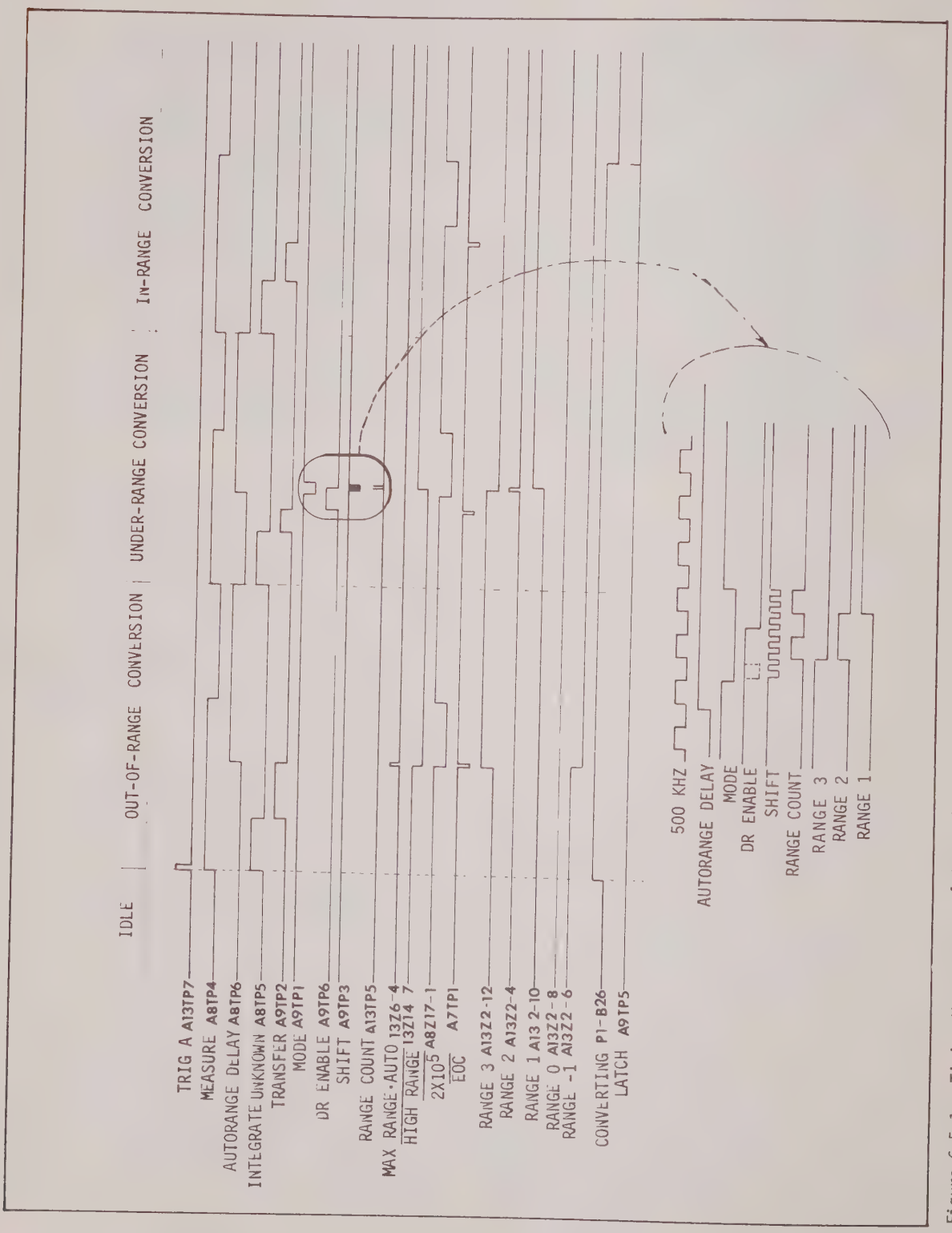

Figure 6.5-1. Timing Waveforms - Autoranging cycle

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6.6 REGISTER AND STORAGE (A9) (Dwg. 55-1003)

6.6.1 General.

Register and Storage Module A9 contains the logic elements comprising the counter, shift register, and storage of measured data, as well as the logic elements for the following functions:

(a) Decode the shifted measured value when in auto-ranging mode to enable down ranging;

(b) Change the unit of least count from X100 to X1 when a slope change is required;

(c) Store the appropriate polarity value for display.

6.6.2 Phase 2 Counting (Measurand Integration).

a. The COUNT pulse train, connected at A9P1-1, is applied directly to the X1 decade (z3) and through the logic control gates of Z21 and Z20-6 to the X100 decade (Z9) of the counter. Control of the counter decade through which the count accumulates is accomplished by the states of flip-flops Z22, Z23, and Z25-14. During Phase 2, the output of Z22-2 keeps Z3 and Z6 (the two lower decades of the counter) in reset condition. At the same time, the action of the Z21 gates connect the count to Z9, thus accumulating the counts at units of X100 in the three higher decades.

b. Overflow of Z15 is sensed by the change in output level of Z18-5, and generates the 1×10^5 indication at A9P1-20. Note that this represents 1000 counts during which the input controls the charging of the integrating capacitor at the fast slope rate during Phase 2 of the A/D cycle.

6.6.3 Reference Integration Counting.

a. Unless there is a SLOPE CHANGE high level input at A9P1-22, the counting will begin in Phase 3 as for Phase 2, at a X100 unit count. When a SLOPE CHANGE input occurs, the flip-flops Z23, Z22 and Z25 are cleared. The high level at Z22-2 results in the enabling of Z3 and Z6 as counters at X1 unit counts for Phase 4 operation.

b. After a SLOPE CHANGE, the count input to Z9 occurs at the overflor of Z6, as required for full 5-decade counting. The first four counts are suppressed to equal the analog offset provided at the comparator input. (See A/D analog discussion.)

c. Flip-flops Z23-3, Z23-5, and Z22-5 monitor the overflow at Z6-11, so that if in Phase 4 the X1 count exceeds 800, there will be a shift back to high rate counting (see chapter 5).

6.6.4 Transfer and Down Range Enable.

a. When, at the end of Phase 4, the TRANSFER signal at A9P1-B is a negative-going transition, the count in the counter is transferred to the shift register (Z2, Z5, Z8, Z11, Z14, and Z17). The wired OR gate connected to A9P1-X (DR ENABLE) senses the output of the shift register two higher decades. If all of the following inputs are low level, then a DR ENABLE command (high level) is transmitted.

Z24-8 (Inverted AUTO; AUTO is high when in Auto-ranging)

LOW RANGE (If already at lowest range, down ranging is not enabled)

A14-10, -11, -12, -13 } Signifying a zero decimal value in the 5th decade

A17-11, -13 } Signifying a zero decimal value in the 6th decade

b. In conjunction with the logic sensing in Module A8, when a down range shift is required, MODE and SHIFT signals at the input to A9 cause the values in the decade registers to shift up 4 bits at a time. The shifted values may then be sensed, as before, to determine whether another down range shift is required.

c. At the end of a conversion, after auto-ranging to a correct range if selected and required, the values in the shift register are transferred into latches Z1, 4, 7, 10, 13, and 16 by the action of LATCH command at A9P1-5.

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6.7 RANGE (A13) (Dwg. 55-1007)

6.7.1 General.

Range Module A13 generates a number of signals determining the range for the display as well as for the control of the signal conditioning. These include:

(a) Developing range signals that control the decimal point display, and that identify the decade range of the conversion to remote users of Model 7500 data;

(b) Developing range control signals for internal selection of gain or attenuation by measurand conditioning circuitry (Range A, B, and C);

(c) Shifting range in response to logic command;

(d) Developing trigger control signals, including decoding of internal and external trigger selection commands.

(e) Controlling REMOTE/LOCAL selection of programming.

6.7.2 REMOTE/LOCAL Control.

Selection of remote programming of all ranges and functions is enabled by the cleared state of flip flop Z13-9. Model 7500 DMM powers up in the LOCAL state (preset), and alternate activations of the front-panel pushbutton discharge C3 into the LOCAL SELECT input to toggle the state between LOCAL and REMOTE. A high level on REM PROG SEL from the interface clears Z13-9, and overrides the LOCAL SELECT input. This action locks out the front panel controls until enabled by a low level on REM PROG SEL or overridden by one of the remote lockout signals. (See para. 1.4.12.1).

6.7.3 Range Decade & Control Signals.

a. One of six range decades or autorange may be selected from either remote or local sources. Module A13 decodes these selection signals to preset range counter flip-flops A, B, and C, and autorange control flip-flop Z7-9 in diode matrix Z9. The A, B, and C levels in flip-flops Z5 and Z7 are then translated into 6 mutually exclusive decade ranges, -1 to 4, by the BCD-to-Decimal element Z3. The maximum range is limited to 1K, except in kilohms, by gates Z14 and Z14-11. Table 6.7-1 summarizes the translations performed in this sequence.

b. Remote range programming capability depends upon the condition of control signals GRA, and STROBE RANGE, as well as the state of LOCAL/REM flip-flop Z13-9. When GRA is set high, then range may be selected only by local programming. When GRA is low, the selection of local or remote programming is determined by the state of LOCAL/REM flip-flop as described in para. 6.7.2. When in LOCAL, pushing a front panel range switch or the AUTO switch connects RANGE ENABLE (from A13P2-7) to the appropriate local select input line. Propagation through diode matrix Z9 routes the signal to appropriate preset and clear inputs of the range counter and AUTO flip-flops. Tri-state buffers Z8 and Z11 multiplex either the local or the remote selection pulses to the single diode matrix. When in REMOTE, the levels on RP Bus lines 1 through 6 are transferred through the diode matrix to the flip-flops only upon receipt of a high level on the STROBE RANGE line, A13P2-17 (see chapter 3).

Table 6.7-1

Active RP Bus	$\overline{\text{LOCAL SELECT}}$	Range Control A	B	C	Z3 Output	Front Panel Light
6	4	0	0	0	Range 4	10K
5	3	1	0	0	3	1K
4	2	0	1	0	2	100
3	1	1	0	1	1	10
2	0	0	1	1	0	1
1	-1	1	1	1	Low Range	.1
Range Strobe Only	Auto	X	X	X	-	Auto

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6.7.4 High Range Decoding.

a. In auto-ranging an out-of-range value over 200,000 counts will cause the Model 7500 to select the maximum range if not already at maximum range. Moreover, the maximum range for kilohms measurements is 10K, whereas it is 1K for all other measurements. The logic circuitry for these decisions is part of Module A13. The command to select the maximum range, MAX RANGE at A13P2-B, is gated in Z6-4 with the auto-ranging signal and is decoded in gates Z14-12 and Z14-9 into the correct control signals for either 1K or 10K range. For kilohms measurement, X is high at A13P1-N, and output of Z14-12 will be low. This causes each range flip-flop to set up the low level on A, B, and C, and a 10K range results. For non-kilohms measurements, X is low, and Z14-9 is low. This sets up a high level on A and a low on B and C, resulting in a 1K range.

b. Operation at the high range is indicated by a low level at the output of Z14-7 and at A13P2-22 for use in the decision circuitry of module A8. Input at Z14-6 senses a range of 10K when in K function, while Z14-5 senses a range of 1K when not in K function.

6.7.5 Trigger Control.

a. Arming, flip flop Z13 is preset to ARM by a low pulse on the ARM signal at A13P2-L, and clocked back to DISARM by the end of the following CONVERT signal at A8P2-Y after inversion through Z12. Thus, is armed and TRIGGER is high at A13P2-F, then the clocked Z13 will generate a TRIG A signal when the CONVERT enable is received after a prior conversion. If ARM is continuously low, all TRIGGER or internal rate pulses are transmitted to TRIG A.

b. Figure 6.7-1 is a simplified schematic showing the connections made via the front panel when the control is in the internal rate range of the panel-mounted potentiometer, R9. The Timer Z1 rate is determined by the setting of R9, and the timer output, Z1-3, is connected in the wired OR input to gate Z6-8.

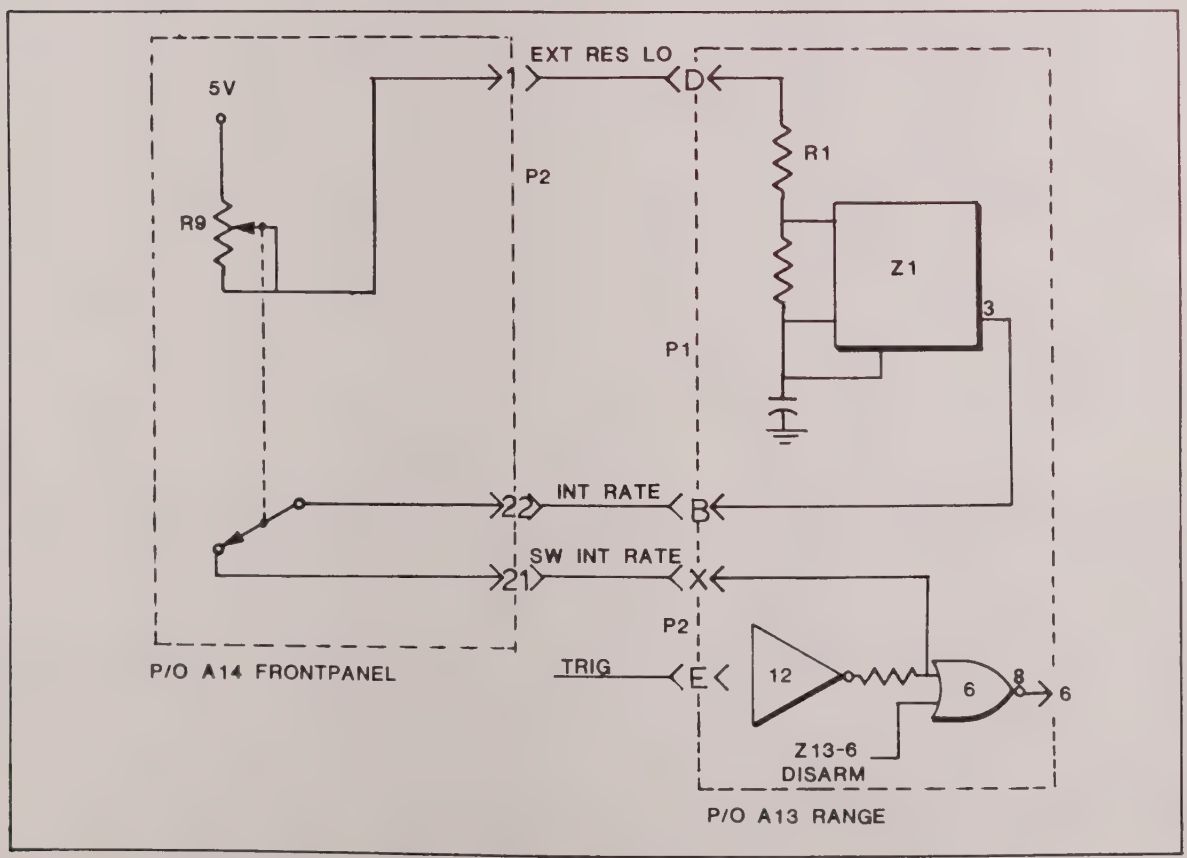

Figure 6.7-1 Trigger control from front panel, Simplified Schematic

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6.8 DISPLAY (A16) (Dwg. 55-1001)

6.8.1 General.

The Display Module A16 is mounted directly behind the front panel. It contains three plasma display components:

(a) A 3-digit unit, SP-353 (DS3)
(b) A 2-digit unit, SP-352 (DS2)
(c) A 1-digit unit, SP-351 (DS1)

DS2 and DS3 are full decade units, while DS1 provides for a polarity indicator and only digits "0" or "1". Each display unit has provision for decimal point activation and display.

6.8.2 Drivers.

a. The decimal digits in each display are formed by combinations of seven-segment elements selected by decoder-drivers Z1 through Z6 that translate the BCD-coded values from the Register and Storage Module A9.

b. An $\overline{\text{OVERLOAD}}$ command is connected at Z1 pin 5 and in chain from pin 4 to successive drivers so that all decimal digits are blanked in OVERLOAD. In OVERLOAD, the value transferred is all zeros so that the Display is all blank, even though only leading zeros are blanked by the internal logic of the IC. Note that the decimal point and polarity sign (if enabled) are not affected by the overload display indication.

6.9 PROGRAM & STORAGE (A12) (Dwg. 55-1006)

6.9.1 Function Overview (Figure 6.9.1-1).

The Program and Storage assembly receives signals from remote source or from front panel operations and decodes these in its digital logic to set control levels on output lines that configure the Model 7500 for:

(a) The measurand signal conditioning
(b) The reference input signal conditioning
(c) The conversion time interval, and
(d) The selection of filter.

Assembly A12 also generates control signals that activate the front panel lights indicating the operational mode selected by the programming and status-indicating signals for remote use.

6.9.2 $\overline{\text{PROGRAM BUSY}}$.

a. Assembly A12 includes circuitry that generates a $\overline{\text{PROG BUSY}}$ signal, when in remote control, that remains at low level for a minimum of 40 milliseconds starting when a program change is made, and which prevents the start of a conversion. Figure 6.9.2-1 is a simplified schematic of that portion of the A12 circuitry that generates the $\overline{\text{PROG BUSY}}$ signal.

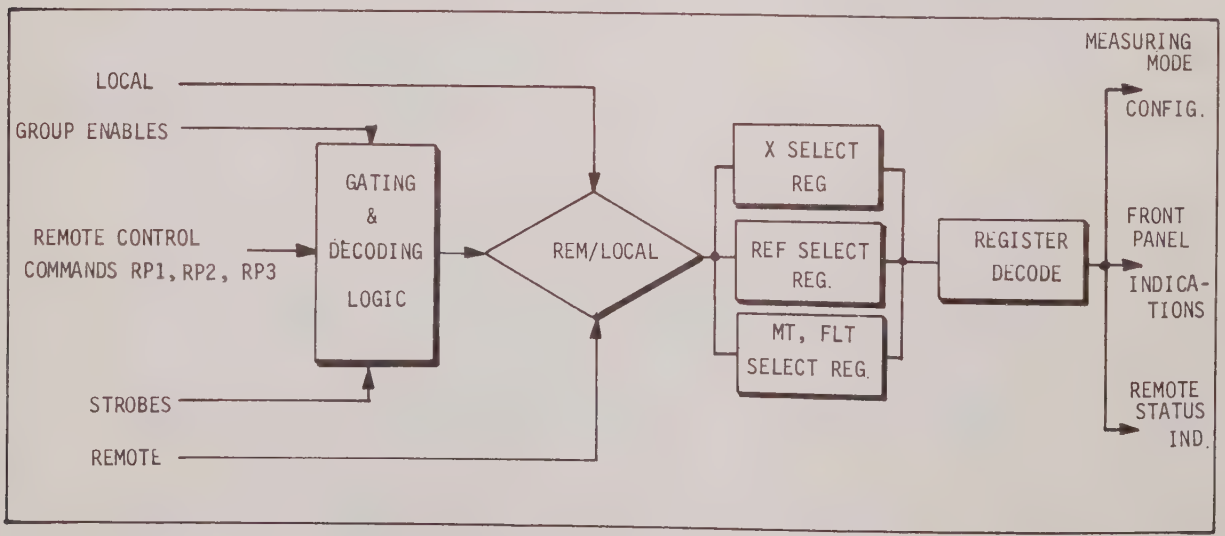

Figure 6.9.1-1 Program and Storage Function, Overview

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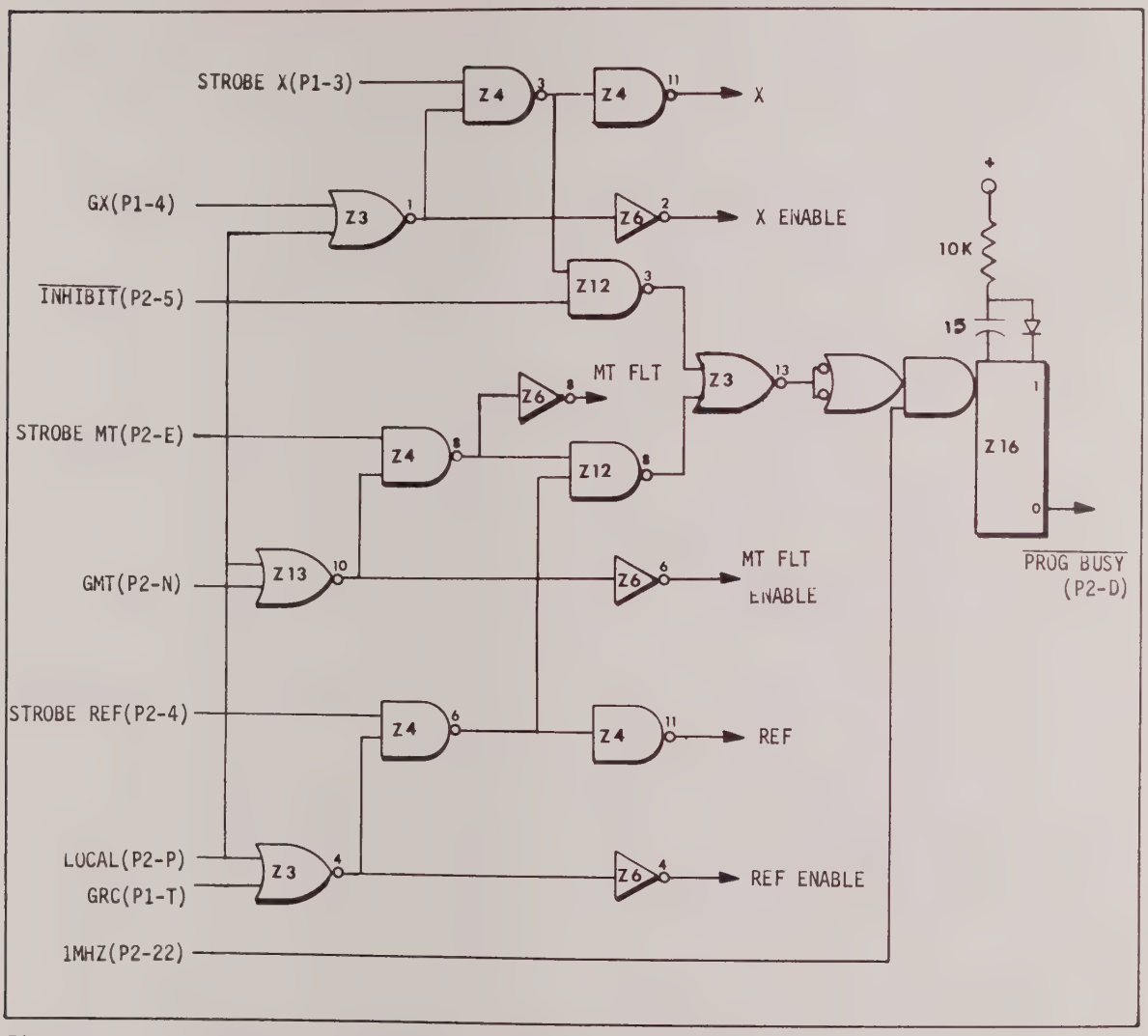

Figure 6.9.2-1 PROGRAM BUSY signal generation

b. As shown in figure 6.9.2-1, the $\overline{\text{PROG BUSY}}$ signal is generated by retriggerable delay on-shot Z16, clocked by the 1 MHz input through A12P2-22. The one-shot is triggered when an input to NOR gate Z3-11 is at high level. This condition is satisfied by any one of the following:

(a) A low level at A12P2-5, $\overline{\text{INHIBIT}}$, indicating a Range Strobe in REMOTE while GRA is low

(b) A high on STROBE REF and low levels on A12P1-1 (GRC) and on A12P2-P (LOCAL)

(c) A high on STROBE MT and low levels on A12P2-N (GMT) and A12P2-P (LOCAL)

(d) A high on STROBE X and low levels on A12P2-U (GX) and on A12P2-P (LOCAL)

c. Flop Z16 will remain in "1" state until the capacitor (15μF) is charged up to the reset level. The time constant of RC = $10^4 \times 15 \times 10^{-6}$ = 150milliseconds provides a time interval of about 40 milliseconds before its state changes. During that time the program may be changed, removing the logic conditions above. When next the conditions are

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satisfied the 40 msec delay is restarted. If still in progress, it will initiate a 40 msec time after the last condition is satisfied.

6.9.3 Program Storage.

a. The two D-type flip flops Z1 set up the levels that determine the measurand signal conditioning selection. DC, AC, Resistance, or TEST. The Z1 states are decoded in NOR gates Z7. The inputs, flip flop states, and outputs are summarized in Table 6.9.3-1, MEASURAND CONTROL. Note that local select inputs are actuated by pushbuttons only when in LOCAL, while the RPB inputs are effective only in REMOTE in conjunction with the X strobe pulse.

b. The two D-type flip flops Z2 set up the levels for control of the reference signal conditioning selection: EXTERNAL DC, AC, RESISTANCE or INTERNAL. The inputs, outputs, and flip-flops states for this channel are included in Table 6.9.3-2, REFERENCE CONTROL. The RP Bus actuates this circuit when in REMOTE and STROBE REF is transmitted.

c. The two flip-flops Z5 control MEASUREMENT TIME selection, as indicated in Table 6.9.3-3, while Z15 controls the filter selection as indicated in Table 6.9.3-4. Both MEASUREMENT TIME and FILTER selection are activated by STROBE MT in REMOTE operation. Note that filter selection is conditioned upon whether AC is selected for the measurand. (Note that STROBE MT pulse controls both filter and measurement time selection. Therefore it is necessary to set up both with the RP Bus controls before strobing.)

6.10 POWER SUPPLIES (A15) (Dwg. 55-1012)

6.10.1 General.

a. Module A15, the main rear panel assembly, contains the subassemblies to develop both isolated and non-isolated power supplies. Module A15A1 assembly contains the guarded circuitry for isolated dc powering of the signal conditioning assemblies and the A/D Converter, including +18 volts for relays and the oven heater, ±30 volts for the dc and ac signal conditioning amplifiers, ±15 volts for the general purpose analog circuits, and -5 volts for isolated digital circuitry. A separate section A15A1Z8 and associated circuits develop the isolated 30 volts which operate the kilohm measurement current source.

b. The A15A2 assembly contains the filtering and regulation circuits for all the non-isolated digital circuits, displays, and interfaces (chassis ground referenced).

6.11 FRONT PANEL (A14) (Dwg. 55-1010)

The Front Panel assembly, Module A14, contains the input binding posts; switch and light assemblies for the front panel selection and display of range, measurement time, measurand signal conditioning, and reference signal conditioning; switch controls for power and filter; and switch and variable rate control for trigger rate. Lamps in the pushbuttons are replaceable from the front without the need for special tools or fixtures. Pull square buttons straight out to remove. Then remove cap from carrier. Be sure wire leads are straight and located on contact springs. Trim leads flush, etc.

6.12 AC SIGNAL CONDITIONING (A4)

6.12.1 AC Signal Conditioning. (OPTION AC1)

a. When AC voltage measurement option is specified, module assembly A4 is installed in the DMM 7500. The operation of A4 together with DC voltage conditioning module assembly, A5, conditions the AC input by full wave rectification and by scaling it so that its average value is calibrated in terms of the rms value of an equivalent sinewave. The AC signal conditioning module A4 schematic is shown in Data Precision drawing 55-1009, reproduced and included in the reference schematics at the back of this manual.

b. As shown in the schematic, the input AC voltage is capacitive coupled through C1 (0.15 uF) to the first stage, operational amplifier, Z1. Depending upon the feedback impedance set up by the action of range-controlled relays K1 and K2, the input amplifier stage Z1 gain is .001755, .01755, .1755, or 1.755. This results in an ac output voltage of 10V peak at maximum input on each range.

c. The output of Z1 is capacitively coupled through C16 (68 F) to both Z2 and Z3. The amplifier Z2 and its circuitry form a half-wave rectifier with a gain factor of 2, and its output is an input to Z3 at an equal gain with the sinewave input to Z3 from stage Z1. The sum of the half-wave output of Z2 and the full sine wave is illustrated in figure 6.12.1-1.

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Table 6.9.3-1 MEASURAND CONTROL

LOCAL SELECT INPUTS	RP SELECT INPUTS	Z1-5	Z1-9	SELECTED (HIGH) X OUTPUT
X	NONE	1	1	A12P1-2
XDC	BUS 1	0	1	A12P1-B
XAC	BUS 2*	0	0	A12P1-C
TEST	BUS 3	1	0	A12P1-E

*Also selected by combinations of BUS 1 & BUS 3 or BUS 2 & any other BUS.

Table 6.9.3-2 REFERENCE CONTROL

LOCAL SELECT INPUTS	RP SELECT INPUTS	Z2-5	Z2-9	SELECTED (HIGH) REF OUTPUTS
REF	NONE	1	1	A12P1-W & P1-Z
REF DC	BUS 3	0	1	A12P1-X & P1-Z
REF AC	BUS 2*	0	0	A12P1-Y & P1-Z
M.T.	BUS 1	1	0	NONE

*Also selected by combinations of BUS 1 & BUS 3 or BUS 2 & any other BUS.

Table 6.9.3-3 MEASUREMENT TIME CONTROL

LOCAL SELECT INPUTS	RP SELECT INPUTS	Z5-5	Z5-9	SELECTED (HIGH) MT OUTPUTS
1ms	NONE	1	0	A12P2-6
8ms	BUS 1	0	0	A12P2-L
64ms	BUS 2	0	1	A12P2-H

Table 6.9.3-4 FILTER CONTROL

LOC. SEL FILT.	LOC. SEL UNFILT.	XAC	STROBE MT. RP BUS 3	A15-5	FILT. Z15-9
0	1	0	1	1	1
1	0	X	0	0	0
0	1	1	1	1	0

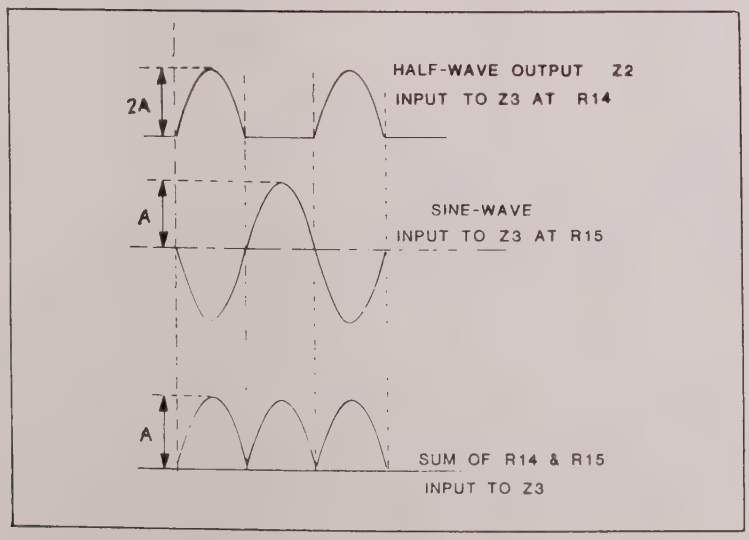

Figure 6.12-1

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The output of Z3 is inverted, filtered, and scaled by a factor of 158.22/25 = 6.32889, and filtered by the active two-pole filter network stage of Z4. The gain of this stage results in a maximum dc output of 20V for maximum input on all except the 0.1 Range where the output is 2V. The resulting DC voltage is then an input to the DC voltage conditioning module, A5, where it is further scaled by gain of either 1 or 10 according to whether LOW RANGE is active and becomes the measurand A/D input for Phase 2 of the quadraphasic conversion. Table 6.12.1-1 summarizes the AC Range selection relay action.

6.13 OHMS SIGNAL CONDITIONING (A2) (Option)

6.13.1 General.

a. Ohms Signal Conditioning option assembly A2 is installed to add the capability for resistance measurement to the Basic Model 7500 DMM. The function of this module is to develop a calibrated sourcing current to be applied to the unknown resistance, generating a dc voltage whose value can be measured and scaled in kilohms by the remaining functions of the Model 7500.

b. Figure 6.13-1 is a simplified schematic of the detailed reference schematic, drawing 55-1010, in Chapter 9. The relay-selected precision resistance, R_S, determines a standard reference current, I_S, for the selected range such that one volt will be generated for each kilohm of resistance, R_X.

c. The block diagram of figure 6.13-2 illustrates the combined operation of A2 Ohms Signal Conditioning, and A5, DC Signal Conditionin, in developing the dc volt input to the A/D. Selection of Ohms Signal Conditioning by the local or remote programming results in a high level X control to A5 that is opto-isolated into the ISO OHMS control to A2. Relay K4, operated by ISO OHMS, connects the sourcing current to the front panel terminals.

6.13.2 Circuit Features.

a. Operational Amplifier Z2 is connected as a constant current generator, and the current amplitude is limited by the resistance selected by isolated range control signals.

b. Diode CR8 and transistor Q5 form a protection against excessive voltage; Q5 has a breakdown potential of 400V; while Q6, Q7, and Q8 provide clamp circuits at the input to Z1.

c. Potentiometer R13 is adjusted for a voltage of 6.2 vdc at TP2, while potentiometers R2, R4, and R6 are adjusted so that the selected standard resistances (R_S in figure 6.13-1) are 62K, 620K, and 6.2M, respectively. R1 is 6.2K. Thus, at the input to Z1,

$$6.200000 = I_S \times R_S$$

So that I_S = 1mA (R1 in circuit)
= 100μA (R2 in circuit)
= 10μA (R4 in circuit)
= 1μA (R6 in circuit)

When K3 operates, the voltage across the standard resistor is reduced to 0.620000V, resulting in a current of I_S = 0.1μA for the 10K RANGE.

Table 6.12.1-1

AC RANGE RELAY SELECTION

RANGE	RANGE CONTROL A	B	C	(A5) RELAY CONTROLS LOW RANGE	K4	(A4) RELAY CONTROLS K1	K2	GAIN FACTORS (A4)*	(A5)**
10K	0	0	0	0	1	0	0	X	X
1K	1	0	0	0	1	0	0	1	0.01
100	0	1	0	0	1	1	0	1	0.1
10	1	0	1	0	1	0	1	1	1.0
1	0	1	1	0	1	1	1	1	10.
0.1	1	1	1	1	0	1	1	10	10.

X = Not Applicable

* $\frac{V_{OUT}\ DC}{V_{IN}\ RMS}$

** $\frac{V_{OUT}\ DC}{V_{IN}\ RMS}$

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7 MAINTENANCE

7.1 GENERAL

Chapter 7 contains information for the routine preventive maintenance and the corrective maintenance, when necessary, for Model 7500DMM. Only qualified repair personnel should attempt to perform the diagnostic procedures and to make the designated repairs and replacements. A thorough understanding of the principles of operation as described in Chapters 5 and 6 are prerequisite for effective and efficient troubleshooting and repair.

7.2 PREVENTIVE MAINTENANCE

7.2.1 "Housekeeping".

At regular intervals, at least once every 6 months, the Model 7500DMM should be cleaned and checked for signs of excessive wear. Remove the top covers; clean with gentle blowing and vacuuming actions. Look for any signs of overheating, such as charred printed circuit boards, discolored components, or solder flow. Refer to the appropriate circuit schematics and perform operational tests involving circuit components that are suspect, if any.

7.2.2 Amplifier Battery Replacement.

Every 12 months the battery in the amplifier assembly in Module A5 should be replaced.

a. Remove the top cover.

b. Lift Assembly module A5 from the main assembly.

c. Loosen the two screws holding the guard cover on the amplifier.

d. Remove the amplifier A5AR1 guard cover.

e. Remove the battery assembly.

f. Install the replacement battery ; observe the polarity conventions as marked on the assembly drawing on page 9-6.

g. Recalibrate the Model 7500DMM as described in Chapter 4 for Zero and Input current.

7.3 CORRECTIVE MAINTENANCE

7.3.1 Maintenance Strategy

Figure 7-1 illustrates a recommended strategy to be used in isolating the cause of an observed malfunction. As shown in the illustration, it is recommended that all external connections of power and signal be checked before assuming any instrument malfunction. Then, by judicious exercise of the front panel controls, it is possible to isolate a large number of malfunctioning components or circuit groups. Only after exhausting the opportunities for troubleshooting the "closed-case" configuration should the covers be removed and open-case troubleshooting be performed.

7.3.2 Closed-case Troubleshooting.

By varying the measurement configuration it is frequently possible to identify the malfunctioning element, or, at least the malfunctioning circuit, before

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removing the cover and making further diagnostic measurements. The following logical summaries are typical of the closed-case analyses that may be applicable. They are presented as guides to the type of thorough evaluations that should be performed before removing the cover and before disturbing internal assemblies.

a. A simple procedure will often isolate the trouble to either the Basic Model 7500DMM configuration, or to one of the installed Options. Operate the instrument in TEST Input Channel and INT Reference Channel. If the displayed value is correct for each RANGE and MT selection, then the Basic configuration is probably functioning properly.

b. In the Basic configuration, vary the RANGE selection. If some results are correct, while one or more of the displayed results is in error, then one may start with the high probability of malfunctioning range circuitry.

c. Vary the MT selection. A correct result on 64 with out-of-spec results on 1ms indicates a problem of adjustment for crossover linearity. See 4.7.4. Correct results on 1ms but not on other MT indicate A/D converter MT selector circuit malfunctions.

d. Connect a variable external voltage input. Observe the display as the input value is varied. Look for faulty segments in the display indicative of malfunctioning display digits, drivers, decoders, etc. in the display circuitry.

7.4 OPEN-CASE TROUBLESHOOTING STRATEGY

7.4.1 Logic Flow Diagrams.

Figure 7-2, in multiple parts illustrates the sequence and decision points that are recommended when prior efforts lead to the requirement for open-case troubleshooting. Essentially, the sequence first checks for proper power supplies, then the range module, program and status module, and dc signal conditioning. The next major test area is the A/D Converter, followed by the automatic ranging circuitry. Beyond this point, continued evidence of improper performance can be traced through the display and storage chain. When complete, the Model 7500 basic configuration is functioning properly and can be used as a "test bed" for checking the installed options.

7.4.2 Test Points.

Test points have been incorporated into the design for optimally efficient troubleshooting and fault isolation.

Table 7-1 lists the testpoints for each assembly. The subsequent text provides a complete description of the symptoms of normal operation expected at the respective points. The description also includes input and measurement configurations that must be set up in order to observe the normal-performance symptoms.

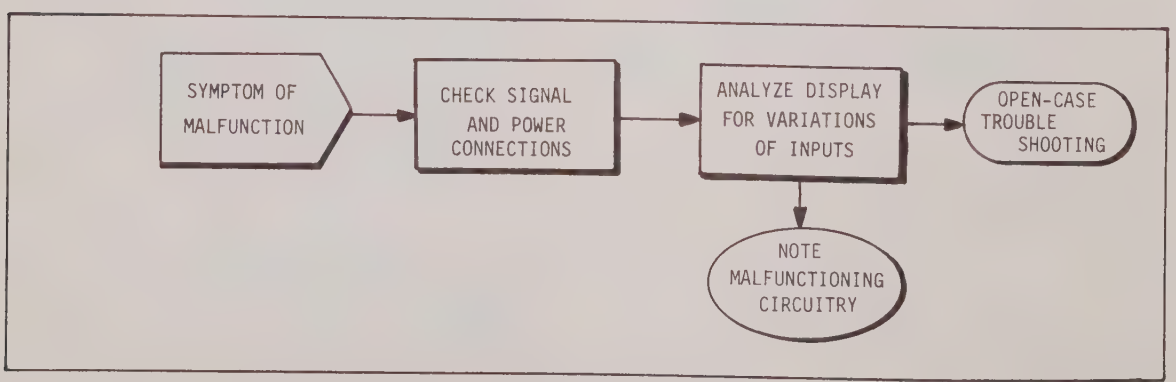
SYMPTOM OF MALFUNCTION
CHECK SIGNAL AND POWER CONNECTIONS
ANALYZE DISPLAY FOR VARIATIONS OF INPUTS
OPEN-CASE TROUBLE SHOOTING
NOTE MALFUNCTIONING CIRCUITRY

Figure 7-1 Closed Case Trouble Shooting

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TABLE OF TEST POINTS

MODULE	TEST	SHORT NAME
A1 Ref. ohms	TP1 TP2 TP3 TP4	HI Amp Output LO Amp Output HI Amp Output LO Amp Input
A2 Ohms Current Source	TP1 TP2 TP3 TP4	+0.62V dc Relative to TP2 Ohms Voltage Reference Point +6.2V dc Relative to TP2 -0 to -.4V Relative to TP2
A3 Ref. AC	TP2 RP2	Rectifier Balance TP's
A4 AC Signal Conditioning	TP1 TP2	Rectifier Balance TP's
A5 DC Signal Conditioning	TP1 TP2 TP3 TP4 TP5	-10V REF & TEST -1V TEST Cond. Ext. REF (ERTP) Amp. Output (V_{IN} COND) Ref. Return TP
A6 A/D Analog	TP1 TP1 TP3 TP4 TP5	Clamp Amp Clamp Amp Z1 Output Z2 Output Integrator Output
A7 Analog Control	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8	$\overline{EOC}$ INT FAST SW INT SLOW SW $\overline{W}$ $\overline{COMPARATOR}$ GND B (Floating Digital) Y +
A8 Programming A/D	TP1 TP2 TP3 TP4 TP5 TP6 TP7	3.84384 MHz Osc (3.20320MHz for 7500E) 1 MHz $\overline{PROG}$ MEASURE INT. UNKNOWN AUTORANGE DELAY DIGITAL GND

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MODULE	TEST	SHORT NAME
A9 Register & Storage	TP1	MODE
	TP2	TRANSFER
	TP3	SHIFT
	TP4	COUNT (x100 INPUT)
	TP5	LATCH
	TP6	DR ENABLE
	TP7	DIGITAL GND
A13 Range	TP1	AUTO
	TP2	LOCAL
	TP3	RANGE A
	TP4	RANGE C
	TP5	RANGE COUNT
	TP6	RANGE B
	TP7	TRIG A

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A1	REFERENCE OHMS OR HI Z DC REFERENCE (RK01-RK06, RDC 01-RDC04)
TP1	Z1-6 REFERENCE HI AMPLIFIER OUTPUT (DC voltage ±12V relative to V_x LO) Amplifier has an input only if REF KΩ is active. Gain from REF HI, TP3 with REF LO grounded is +5.5X for REF OHMS or 1V DC REF configuration, 1X for 10V HI Z DC REF configuration.
TP2	Z2-6 REFERENCE LO AMPLIFIER OUTPUT (DC voltage ±12V relative to V_x LO) Amplifier has an input only if REF KΩ is active. Gain from REF HI, TP3 with REF LO grounded is -4, 5X for REF OHMS or 1V DC REF configuration gain from REF LO, TP4 with REF HI grounded is +5.5X for REF OHMS or 1V DC REF, 1X for 10V HI Z DC REF configuration.
TP3	Z1-2 REFERENCE HI AMPLIFIER INVERTING INPUT. DC voltage equal to REF HI input when REF KΩ is active. Used for calibration of gain.
TP4	Z2-2 REFERENCE LO AMPLIFIER INVERTING INPUT. DC voltage equal to REF LO INPUT when REF KΩ is active. Used for calibration of gain.
A1	100V FS HI Z DC REFERENCE (RDC05)
TP1	ATTENUATOR TAP HI. Reference Hi input attenuated by 10.
TP2	ATTENUATOR TAP LO. Reference Lo input attenuated by 10.
A2	OHMS CURRENT SOURCE (K1)
TP1	+0.62 VOLTS DC RELATIVE TO TP2 FOR 10MEG RANGE. Value is set exactly to calibrate 10MEG range current with 10MEG load from OHMS HIGH to OHMS LOW. Absolute voltage floats relative to V_x LO, or chassis, until OHMS HIGH OHMS LOW are connected to the V_x HIGH and LOW terminals.
TP2	Z1-3 Virtual reference point for ohms current source voltage measurements. Absolute voltage floats.
TP3	"30A+", +6.2 VOLTS DC RELATIVE TO TP2. Value is set exactly to calibrate 1KΩ RANGE current, with 1KΩ from OHMS HIGH to OHMS LOW. Absolute voltage floats.
TP4	Z2-3 UNTRIMMED OHMS REFERENCE TEST POINT. -6.2 to -6.4V DC relative to TP3. Absolute voltage floats.
A3	REFERENCE AC (RAC01-RAC05)
TP1	-RECTIFIER BALANCE TP. A negative half wave rectified waveform isolated through 100KΩ, active only when ac measurand is selected. Used in calibration with TPZ to set the dc rectifier balance ,R17, for zero with zero ac input.
TP2	+RECTIFIER BALANCE TP. A positive half wave rectified waveform proportional to ac input, isolated through 100KΩ. See TP1.
A3	AC REFERENCE SIGNAL CONDITIONING (Option RAC06-RAC10).
TP1	UNFILTERED DC OUTPUT TP. DC proportional to the RMS AC input but not fully filtered to AC components.
TP2	SCALED AC TP. AC input waveform amplitude scaled to 2V RMS for full scale.

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A4	AC SIGNAL CONDITIONING
TP1	-RECTIFIER BALANCE TP. A negative half wave rectified waveform proportional to AC input, isolated through 100KΩ, active only when ac measurand is selected. Used in calibration with TP2 to set the dc rectifier balance ,R17, for zero with zero ac input.
TP2	+RECTIFIER BALANCE TP. A positive half wave rectified waveform proportional to ac input, isolated through 100KΩ. See TP1.
A4	AC SIGNAL CONDITIONING (Option AC2)
TP1	UNFILTERED DC OUTPUT TP. DC proportional to the RMS AC input but not fully filtered of AC components.
TP2	SCALED AC TP. AC input waveform amplitude scaled to 2V RMS for full scale.
A5	DC SIGNAL CONDITIONING
TP1	-10V REF. The basic -10V dc signal used as reference for internal reference and as the 10V test signal. Set exactly relative to reference return, TP5. (TP5 no applicable serial #1-20).
TP2	-1V TEST. The -1V test signal derived from -10V ref. set exactly relative to reference return, TP5. (TP5 no applicable serial #1-20).
TP3	ERTP. Conditioned External Reference. ±11V dc at maximum reference values. DC reference conditioned is at this TP even when INT. REF is active.
TP4	VIN COND. The output of amplifier AR1 is the conditioned input to A/D converter. ±22V dc maximum operating, ±24V dc typical in overload.
TP5	REFERENCE RETURN. The single point ground (mecca) with respect to which all analog signal potentials are measured. (TP5 is offset by 100μV, serial #1-20, use V_x LO as reference point.)
A6	A/D ANALOG
TP1	Z6-1 CLAMPING AMPLIFIER OUTPUT. Normally at -12V approx. saturation level. +.6V or more positive if VIN COND. exceeds the full scale level for the reference in use and is negative.
TP2	Z6-7 CLAMPING AMPLIFIER OUTPUT. Normally at -12V approx. saturation level. +.6V or more if VIN COND. exceeds the full scale level for the reference in use and is positive.
TP3	Z1-6 FIRST AMPLIFIER OUTPUT. During Autozero (Q1) approximately zero. During Q2, VIN COND. X(-0.5). During REF. integration Q3 & Q4 if positive sign output this point has -0.5X ref., if negative sign output this point has zero ± a few millivolts offset.
TP4	Z2-6 SECOND AMPLIFIER OUTPUT. During autozero approximately zero. During Q2, VIN COND. X(+0.5).during REF. integration Q3 & Q4, REF X(0.5) of polarity opposite to VIN COND.
TP5	INTEGRATOR OUTPUT. Isolated by 100Ω to limit effect of capacitive loading by probes, shows triple slope or dual slope waveform with pauses as appropriate for input. Voltage change is approximately 50μV per count, ±11 volts peak for max inputs.

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A7	ANALOG CONTROL NOTE: Low (0) logic level is -5V, high (1) level is -2V to 0V relative to gnd B.
TP1	$\overline{EOC}$. A negative pulse starting when the integrator has passed about 150μV through the autozero baseline in P4. Signals end of the analog conversion process to the unguarded digital circuits.
TP2	INT. FAST SW. A logic level which is high during P1, P2, and P3 except for pauses. It It turns on the FET controlling the fast integrator input (10K resistor) when high.
TP3	INT. SLOW SW. A logic level which is high during P4. It turns on the FET controlling the slow integrator input (1 meg resistor) when high.
TP4	W. A logic level which goes high when a $\overline{START\ CONV.}$ A pulse is received from the unguarded digital circuits, remains high while the A/D is converting, and goes low at the end of the pause following P4. A low level forces the A/D to the autozero state.
TP5	$\overline{COMP.}$ The inverted comparator output. Note: When the comparator is in its active region (typical of P1) this signal is very noisy. This signal is high if the integrator output is more positive than the active threshold of the comparator and low if the integrator output is more negative than the threshold.
TP6	GND B. The guarded section digital reference point. Connected to V_X LOW but isolated from chassis and unguarded digital ground. It is noisier than A5TP5, so don't use for analog measurements.
TP7	Y. A logic level which becomes high during the pause following P2, and remains high during P3 and P4. It becomes low at the end of $\overline{EOC}$.
TP8	+. A logic level which is set at the end of P2 if the ratio of VIN COND. to REF. results in a positive value whether sign display is inhibited or not. It is cleared by $\overline{EOC}$ or W low, whichever occurs first.
A8	PROGRAMMING A/D Logic level low (0) = (V to +0.8V high (1) = +2.4 to +5.5V
TP1	3.84384MHz. The master crystal oscillator for all A/D operations. All clock pulse rates are derived from this frequency by division and/or gating. (3.20320MHz 7500E)
TP2	"1MHz. The master oscillator frequency divided by 4. Actual frequency 960.96KHz. (7500) Used by circuits on PROG & STATUS and interfaces, and further divided in shift timing of autoranging.
TP3	$\overline{PROG.}$ A negative 0.26 μsec. pulse on this line advances the fixed timing program of the guarded section of the A/D. Pulses occur at the end of each pause, the end of P2, and end of autozero recovery (240,000 count).
TP4	MEASURE. A logic level which is set high by a pulse at the start of each A/D conversion cycle whether initiated by a trigger or the end of autorange delay and returned low by the end of autozero recovery (240,000).
TP5	INTEGRATE UNKNOWN. A logic level which is set high at the end of the initial pause and returns low at the end of the pause following P2. Useful as a mux switch flag if autoranging is not used.
TP6	AUTORANGE DELAY. The output of a one-shot which fires after END CONV. is detected if AUTORANGE is selected and the range in use is not the correct one. For dc measurand with filter out the time is nominally 40 milliseconds, otherwise it is 350 milliseconds. During this time the new range is selected, analog settling occurs, and autozero recovery is completed.
TP7	DIGITAL GND. Connected to the non-guarded power supply common point and chassis. Useful for grounding probes while testing other TP's.

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A9	REGISTER & STORAGE
TP1	MODE. A logic level, normally high, which goes low under control of DOWN RANGE ENABLE during autorange delay. While it is low the shift register is enabled to shift right on shift pulses. While it is high shifting is inhibited and parallel transfer of data from the counter to the register is enabled.
TP2	TRANSFER. A level which goes low at EOC or when 200,000 counts indicates overlaod, transferring the data in the counter to the shift register. MODE always should be high at that time.
TP3	SHIFT. One or more bursts of four negative pulses, occurring only while mode is low. Each burst shifts the data in the shift register right by one BCD digit, and is accompanied by down ranging one range. The pulses are approximately 0.5 μsec. wide spaced 0.5μ sec apart.
TP4	FAST COUNTER INPUT. The input to the 100 stage of the counter. During P2 and P3 this point receives pulses at the clock frequency for the selected measurement time. During P4 it receives pulses at .01 times the clock frequency. Following the transfer pulse it again counts at the full clock frequency until the counter contents is 240,000 which ends autozero recovery and the conversion cycle. It is inactive during pauses and during the autozero time between the end of the recovery and the start of a new conversion.
TP5	LATCH. A positive pulse which occurs at the end of a conversion cycle, except when an autorange delay is active. The pulse transfers the data from the shift register to the output latches which control the display.
TP6	DR ENABLE. A level which is high only when in AUTORANGE, not on the lowest range, and the 10,000 through 200,000 stages of the shift register are all zero.
TP7	DIGITAL GND. Connected to the non-guarded power supply common point and chassis. Useful for grounding probes while testing other TP's.

A13	RANGE MODULE
TP1	AUTO. A logic level which is high when autoranging is enabled and low when it is disabled.
TP2	LOCAL. A logic level which is high when all front panel controls are operative and low when remote control is operative.
TP3	RANGE A. A logic level range counter output which is high when either the .1, 10, or 1K RANGE is selected.
TP4	RANGE C. A logic level range counter output which is high when either the .1, 1, or 10 RANGE is selected.
TP5	RANGE COUNT. A positive pulse which occurs during autoranging while MODE is low which causes the range counter to decrement by one range.
TP6	RANGE B. A logic level range counter output which is high when either the .1, 1, or 100 RANGE is selected.
TP7	TRIG. A. A positive pulse or level at this point is generated when the arm flip-flop is set and either an internal or external trigger (as selected by the EXT-RATE switch) pulse or level is applied. A high level here starts a conversion if not already converting and if PROGRAM BUSY is not low.

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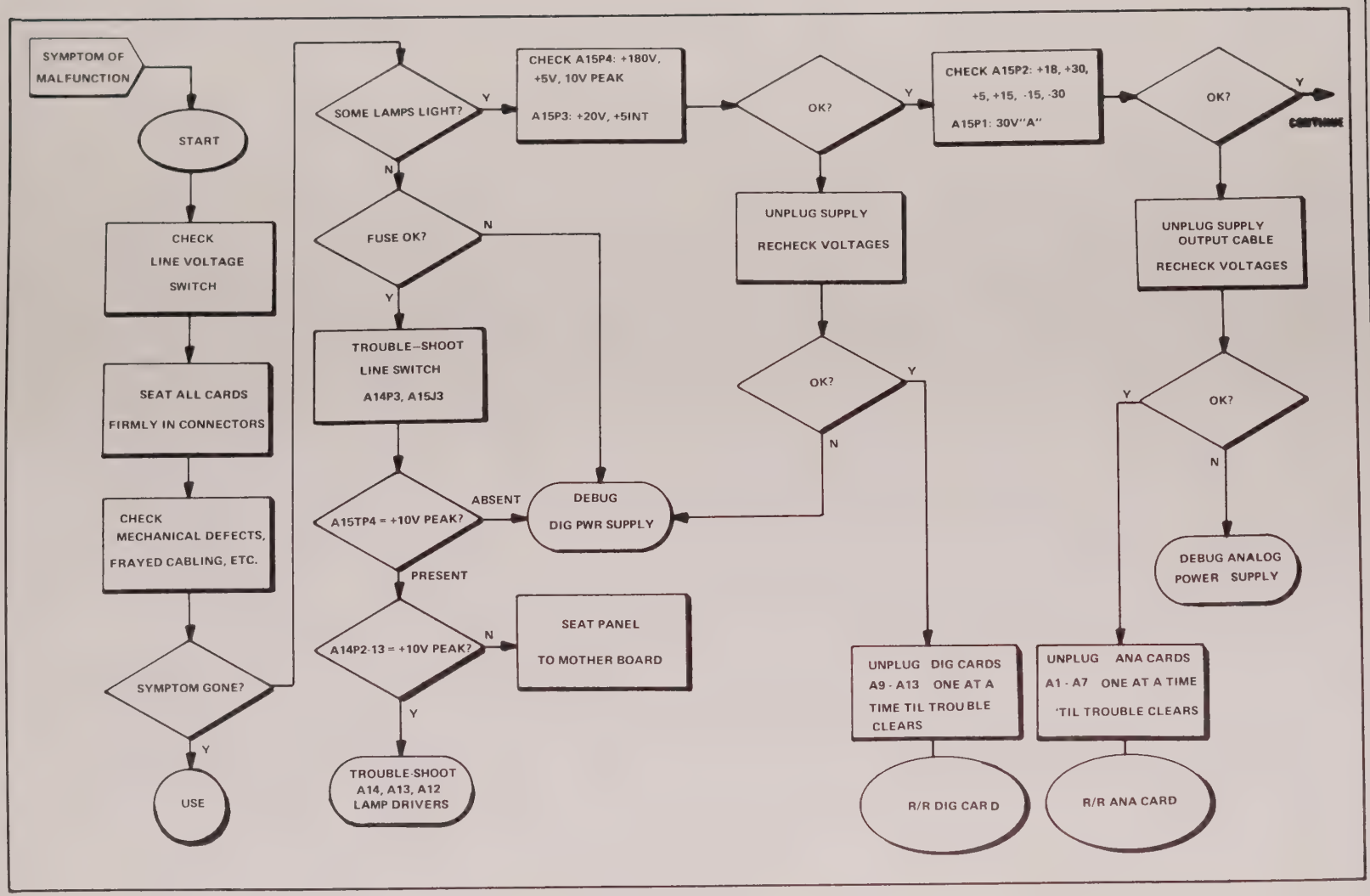

Figure 7-2A Start of Trouble-shooting Strategy

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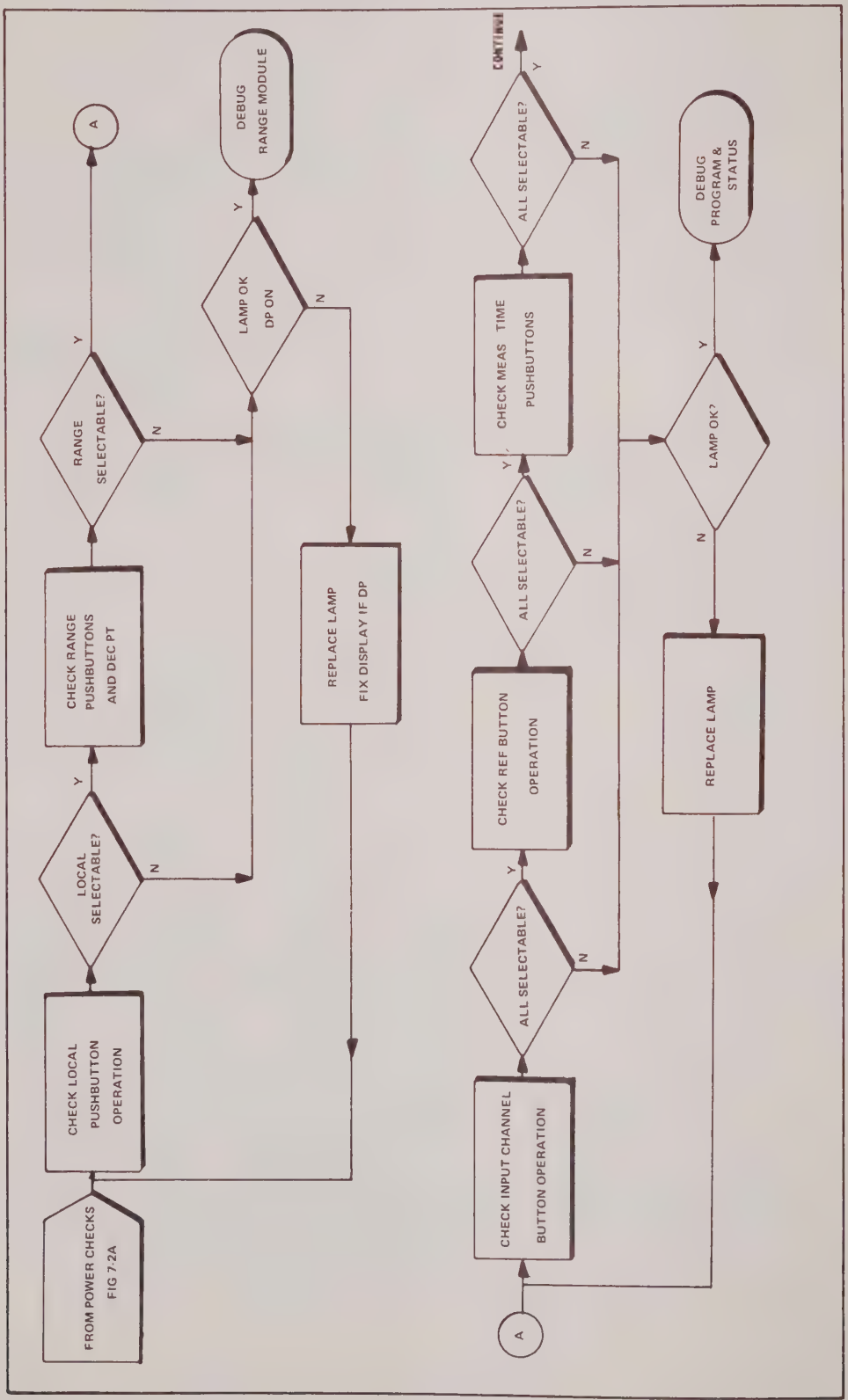

Figure 7-2B Continuation of Trouble-shooting Strategy

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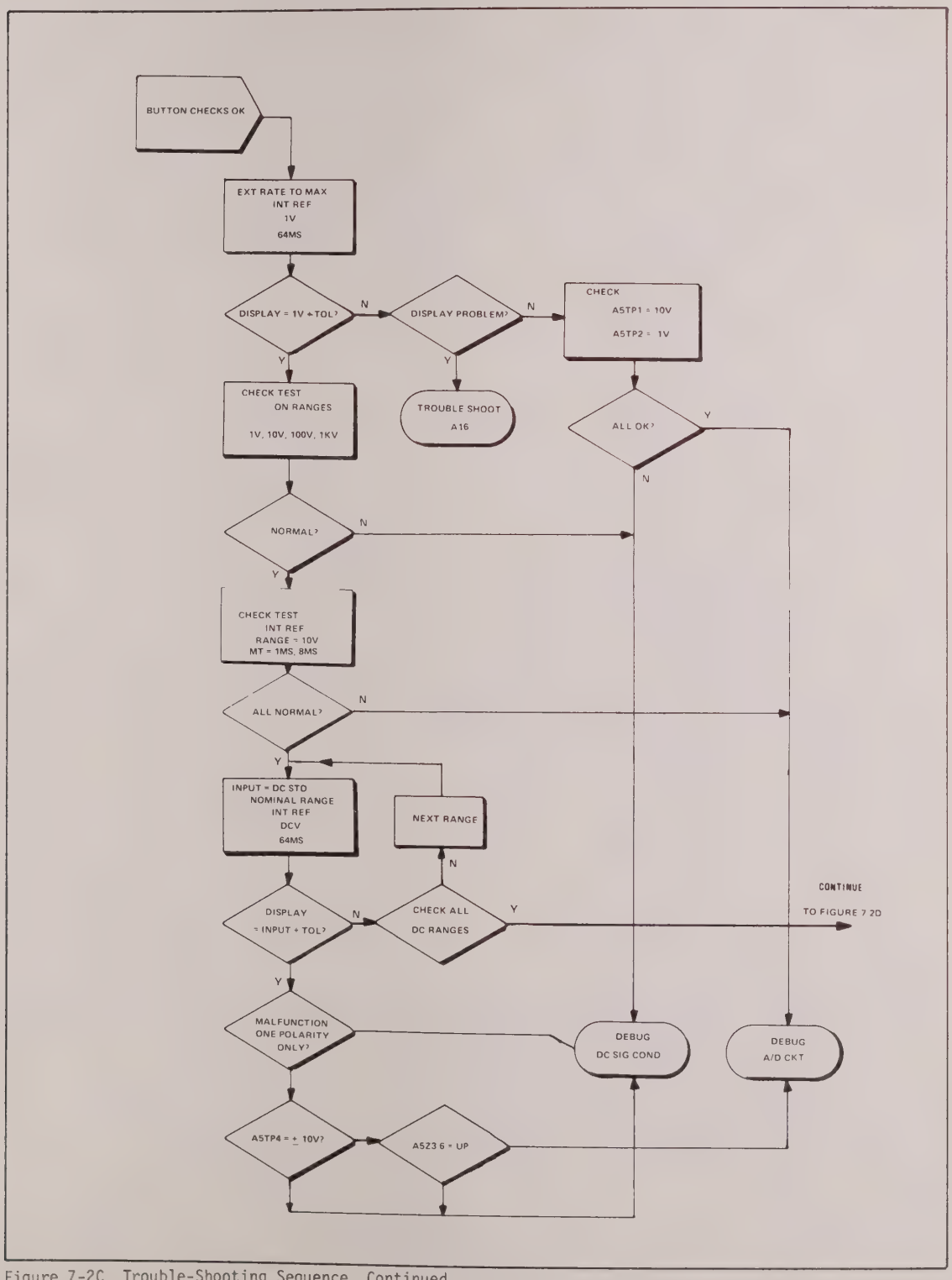

Figure 7-2C Trouble-Shooting Sequence, Continued

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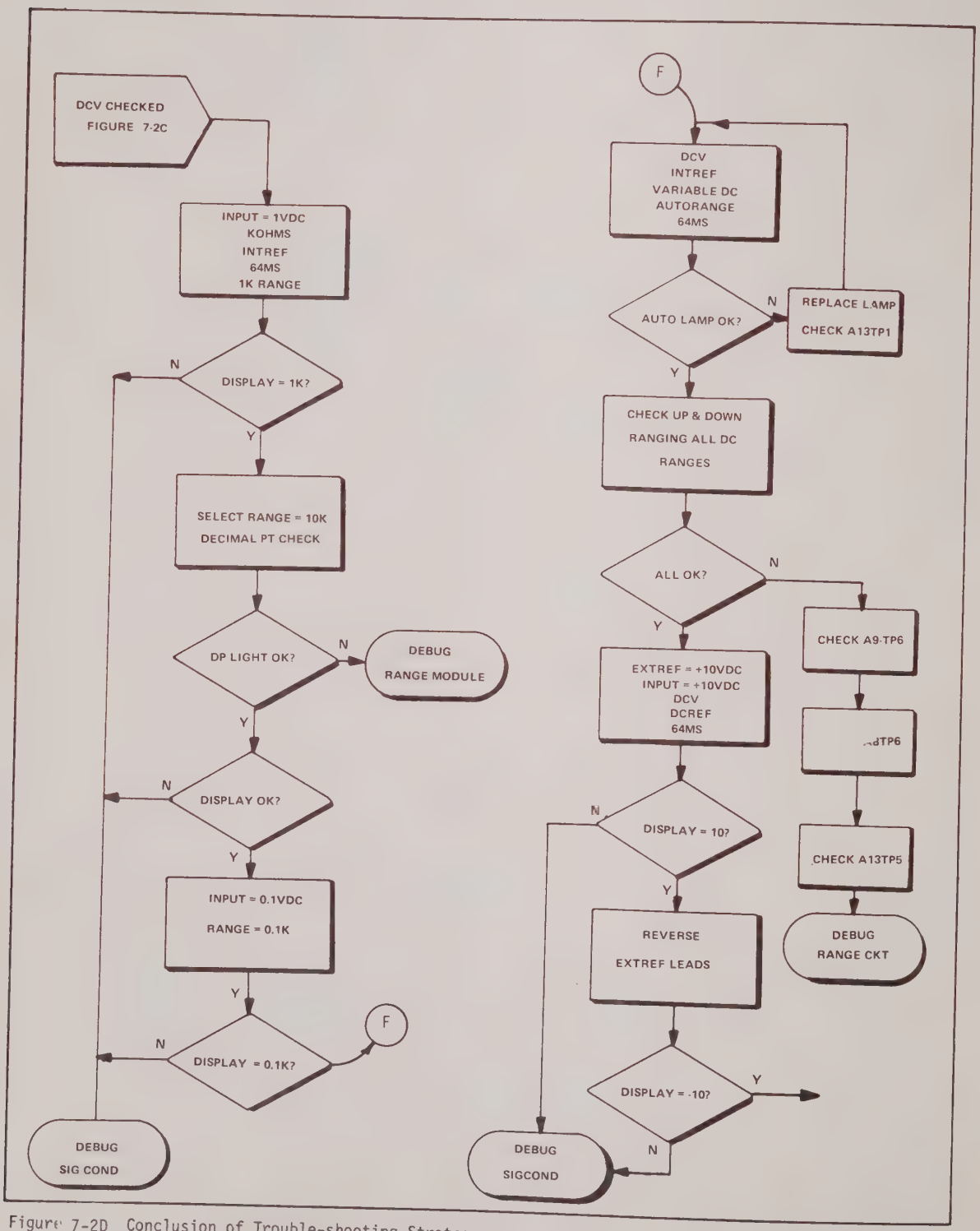

Figure 7-2D Conclusion of Trouble-shooting Strategy

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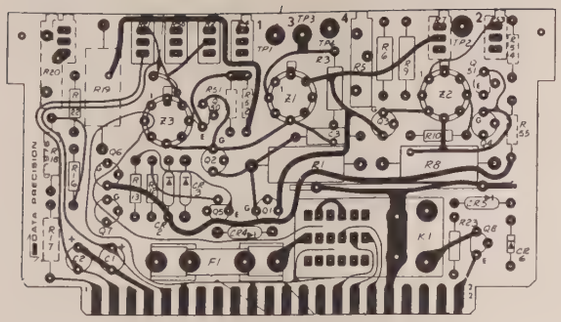
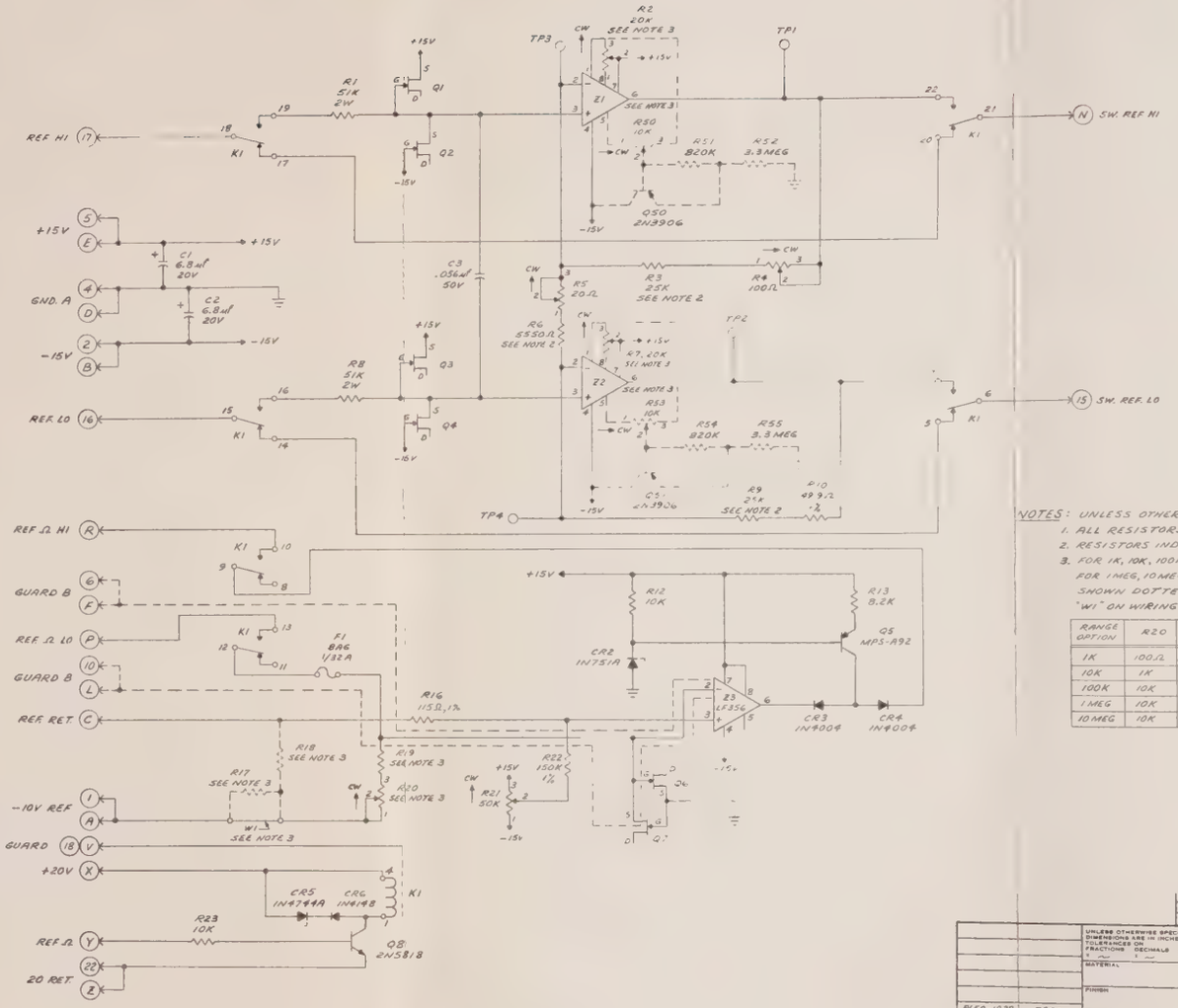


REF. OHMS CONDITIONING P.C. ASSEMBLY (BASIC)
PL50-1029, REV. C

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1,2	CAPACITOR,6.8µf,20V,TANT	23-441005
C3	CAPACITOR,0.056µf,50V,P.C.	23-510020
CR2	DIODE,ZENER,1N751A	24-120073
CR3,4	DIODE,RECTIFIER,1N4004	24-104004
CR5	DIODE,ZENER,1N4744A	24-121103
CR6	DIODE,SWITCH,1N4148	24-110001
K1	RELAY,6 FORM C	25-171005
Q1,2,3,4,6,7	TRANSISTOR,FET,ORN DOT	24-48-1014-10
Q5	TRANSISTOR,MPS-A92	24-240A92
Q8	TRANSISTOR, 2N5818	24-235818
R1,8	RESISTOR,51K,2W,5%,C.C.	22-055139
R3,R6,R9	RESISTOR SET 25K (R3,R9) 5550Ω(R6)	22-58-1012G17
R4	RESISTOR,TRIM,100Ω	22-681002
R5	RESISTOR,TRIM,20Ω	22-681100
R10	RESISTOR,49.9Ω1%,RN55C	22-3449R9
R12,23	RESISTOR,10K,¼W,5%,C.C.	22-021039
R13	RESISTOR,8.2K,¼W,10%,C.C.	22-028228
R16	RESISTOR,115Ω,1%,RN60C	22-371150
R21	RESISTOR,TRIM,50K	22-681009
R22	RESISTOR,150K,1%,RN55D	22-331503
F1	FUSE,1/32A,8AG	25-501010
Z3	I.C.,OP. AMP.,LF356H	24-420356

(SEE PAGE 9-1.1 FOR VARIOUS OPTIONS)



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5%, C.C.
2. RESISTORS INDICATED ARE A MATCHED SET PER S.C.D. 858-1012 G17
3. FOR 1K, 10K, 100K OPTIONS AS SHOWN, AMPLIFIERS (Z1, Z2) ARE OP-07C
FOR 1MEG, 10MEG RANGE OPTIONS: DELETE R2, R7 & ADD COMPONENTS SHOWN DOTTED. AMPLIFIERS (Z1, Z2) ARE BB 3521K. CUT ETCH LINE "W1" ON WIRING SIDE OF BOARD WHEN INSTALLING R17.

RANGE OPTION	R20	R19	R17	R18	S.C.L. 858-1012	OPTION P/N NO.
1K	100Ω	99.60Ω	—	—	GROUP 12	PL50-1037
10K	1K	99.60K	—	—	GROUP 13	PL50-1038
100K	10K	996.0K	—	—	GROUP 14	PL50-1039
1MEG	10K	996.0K	89.1K	10.0K	GROUP 15	PL50-1040
10MEG	10K	996.0K	99.0K	1.000K	GROUP 16	PL50-1041

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN A. Wolk DATE 6.20.74
CHECKED
DESIGNER
ENGINEER
APPROVED
RELEASED
WEIGHT

DATA PRECISION

SCHEMATIC, AI
REF. OHMS CONDITIONING
SYSTEMS DVM

PL50-1029	7500
NEXT ASSY	USED ON
APPLICATION	

SIZE D | 55-1029 | REV A
SCALE ~ | ACCOUNT NO | SHEET 1 OF 1

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THE FOLLOWING OPTIONS USE THE BASIC P/L (PL50-1029)
IN ADDITION TO THE FOLLOWING PARTS FOR EACH OPTION

REF. OHMS CONDITIONING P.C. ASSY
1K FS OPTION (02)
PL50-1037, REV.-

REFERENCE DESCRIPTION	DESCRIPTION	D.P. PART NO.
R2,7	RESISTOR,TRIM,20K	22-681008
R19	RESISTOR,PREC.,9960Ω	22-58-1012G12
R20	RESISTOR,TRIM,100Ω	22-681002
Z1,Z2	I.C.,OP. AMP,OP-07C	24-420007

REF. OHMS CONDITIONING P.C. ASSY
10K FS OPTION (03)
PL50-1038, REV.-

REFERENCE DESCRIPTION	DESCRIPTION	D.P. PART NO.
R2,7	RESISTOR,TRIM,20K	22-681008
R19	RESISTOR,PREC,99.60K	22-58-1012G13
R20	RESISTOR,TRIM,1K	22-681004
Z1,Z2	I.C.,OP. AMP.,OP-07C	24-420007

REF. OHMS CONDITIONING P.C. ASSY
100K FS OPTION (04)
PL50-1039, REV.-

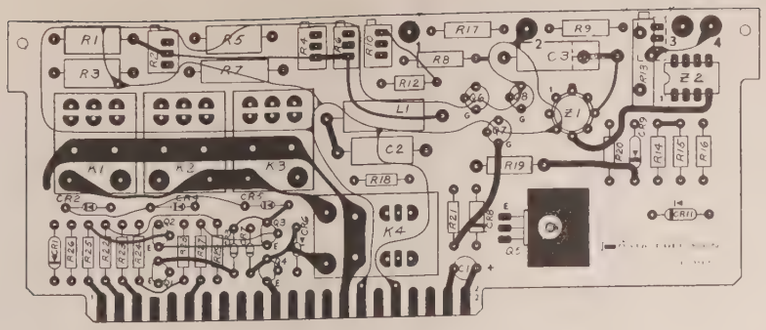
REFERENCE DESCRIPTION	DESCRIPTION	D.P. PART NO.
R2,7	RESISTOR,TRIM,20K	22-681008
R19	RESISTOR,PREC.,996.0K	22-58-1012G14
R20	RESISTOR,TRIM,10K	22-681007
Z1,Z2	I.C.,OP. AMP.,OP-07C	24-420007

REF. OHMS CONDITIONING P.C. ASSY
1MEG. FS OPTION (05)
PL50-1040, REV.-

REFERENCE DESCRIPTION	DESCRIPTION	D.P. PART NO.
R17,18,19	RESISTOR SET,GR.15 89.1K (R17) 10.0K (R18) 996.0K (R19)	22-58-1012G15
R20,50,53	RESISTOR,TRIM,10K	22-681007
R51,54	RESISTOR,820K,¼W,5%,C.C.	22-028249
R52,55	RESISTOR,3.3MEG,¼W,5%,C.C.	22-023359
Q50,Q51	TRANSISTOR,2N3906	24-243906
Z1,Z2	I.C.,OP. AMP.	24-423521

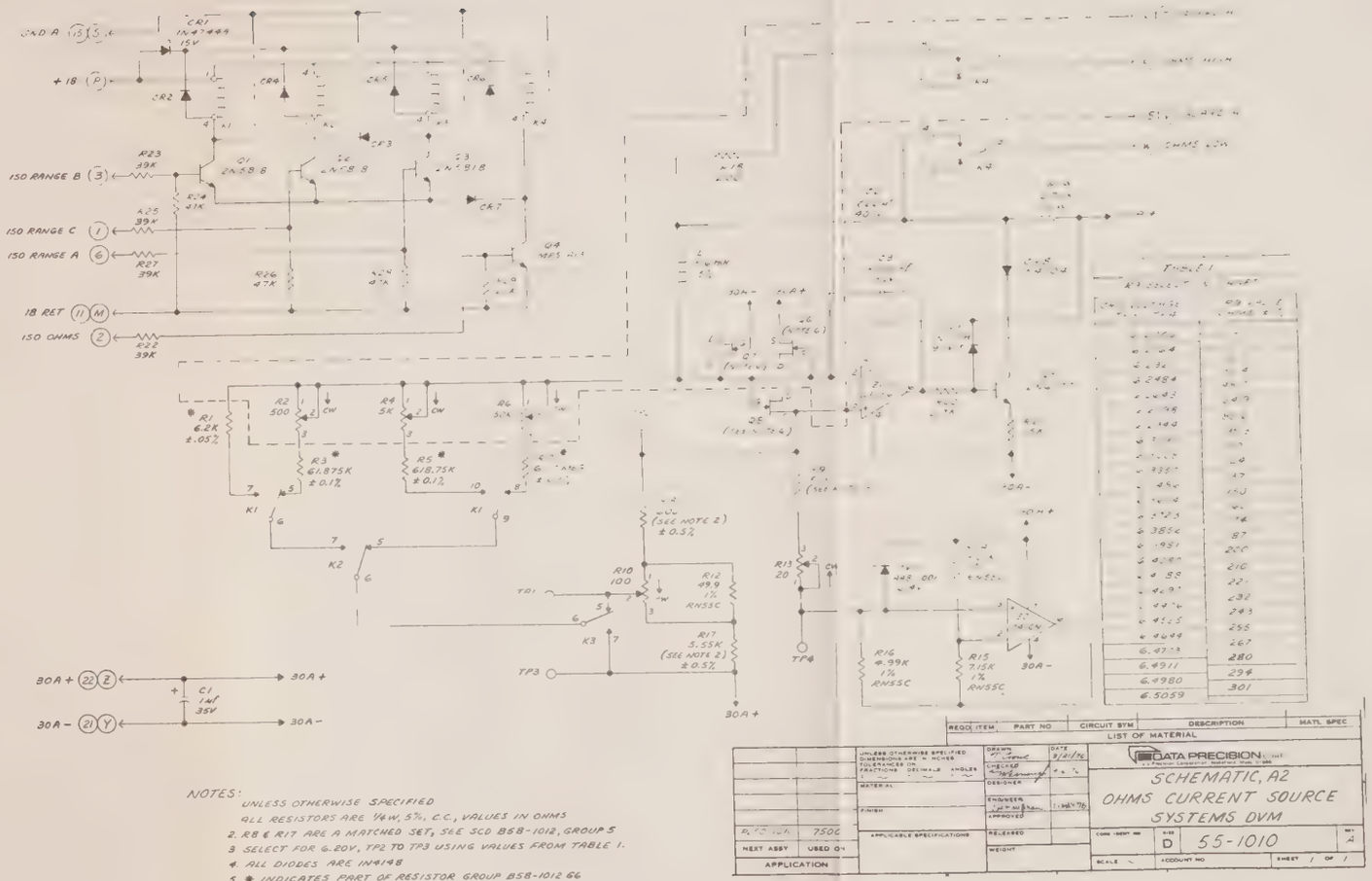
REF. OHMS CONDITIONING P.C. ASSY
10 MEG. FS OPTION (06)
PL50-1041, REV.-

REFERENCE DESCRIPTION	DESCRIPTION	D.P. PART NO.
R17,18,19	RESISTOR SET,GR.16	22-58-1012G16
R20,50,53	RESISTOR,TRIM,10K	22-681007
R51,54	RESISTOR,820K,¼W,5%,C.C.	22-028249
R52,55	RESISTOR,3.3MEG,¼W,5%,C.C.	22-023359
Q50,51	TRANSISTOR,2N3906	24-243906
Z1,Z2	I.C.,OP. AMP.	24-423521



OHMS CURRENT SOURCE P.C. ASSEMBLY
PL 50-1010 REV C

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR,1 mf,35V	23-441001
C2	CAPACITOR,POLYCARB,.022mf,400V	23-510015
C3	CAPACITOR,POLYSTY,3000pf,30V	23-550103
CR1	DIODE,ZENER,1N4744A(15V)	24-121103
CR2 thru CR7	DIODE,SWITCHING,1N4148	24-110001
CR8	DIODE,RECTIFIER,1N4004	24-104004
CR9	DIODE,ZENER,1N4739A(9.1V)	24-121102
CR11	DIODE,REF(6.3V ±.1V,2ms,.005%/°C)	24-48-1001
K1,2,3	RELAY,2 FORM C	25-171002
K4	RELAY, 2 FORM C, HI VOLTAGE	25-58-1014
L1	INDUCTOR, 5.6mH,5%	25-100025
Q6,7,8	TRANSISTOR, FET (ORANGE DOT)	24-48-1014-10
Q1,2,3	TRANSISTOR,NPN,2N5818	24-235818
Q4	TRANSISTOR,DARLINGTON,MPS-A13	24-230A13
Q5	TRANSISTOR,HV,POWER,2N6177	24-226177
R2	RESISTOR, TRIM, 500Ω	22-681003
R4	TRIM, 5K	22-681006
R6	TRIM, 50K	22-681009
R10	TRIM, 100Ω	22-681002
R13	RESISTOR, TRIM, 20Ω	22-681100
R8,R17	RESISTOR SET,GROUP 5	22-58-1012G5
	5550Ω (R17)	
	600Ω (R8)	
R1,3,7,9	RESISTOR SET,GROUP 6	22-58-1012G6
	6200Ω (R1)	
	61875Ω (R3)	
	618.75K (R5)	
	6.17 MEG (R7)	
R9	RESISTOR,FILM,FSV,1% (0 to 182Ω,RN55D BELOW 49.9Ω, RN55C ABOVE 49.9Ω)	
R12	RESISTOR,FILM,49.9Ω,RN55C	22-3449R9
R14	RESISTOR,FILM,3.01K,1%,RN55C	22-343011
R15	RESISTOR,FILM,7.15K,1%,RN55C	22-347151
R16	RESISTOR,FILM,4.99K,1%,RN55C	22-344991
R18	RESISTOR,200Ω,¼W,5%,C.C.	22-022019
R19	270K,½W,5%,C.C.	22-032749
R20	2.7K,¼W,5%,C.C.	22-022729
R21	15K,¼W,5%,C.C.	22-021539
R22,23,25,27	39K,¼W,5%,C.C.	22-023939
R24,26,28	47K,¼W,5%,C.C.	22-024739
R29	RESISTOR,22K,¼W,5%,C.C.	22-022239
Z1	I.C. LF356	24-420356
Z2	I.C. 741CN	24-400741



NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE ¼W, 5%, C.C., VALUES IN OHMS
2. R8 & R17 ARE A MATCHED SET, SEE SCD B58-1012, GROUP 5
3. SELECT FOR 6.20V, TP2 TO TP3 USING VALUES FROM TABLE I.
4. ALL DIODES ARE IN4148
5. * INDICATES PART OF RESISTOR GROUP B58-1012 G6
6. FETS Q6, Q7 & Q8 ARE A48-1014-10

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

DATA PRECISION

SCHEMATIC, A2
OHMS CURRENT SOURCE
SYSTEMS DVM

D 55-1010

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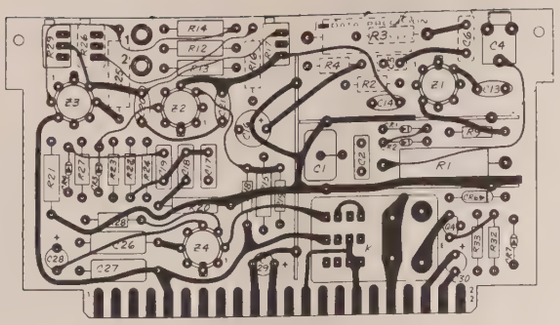
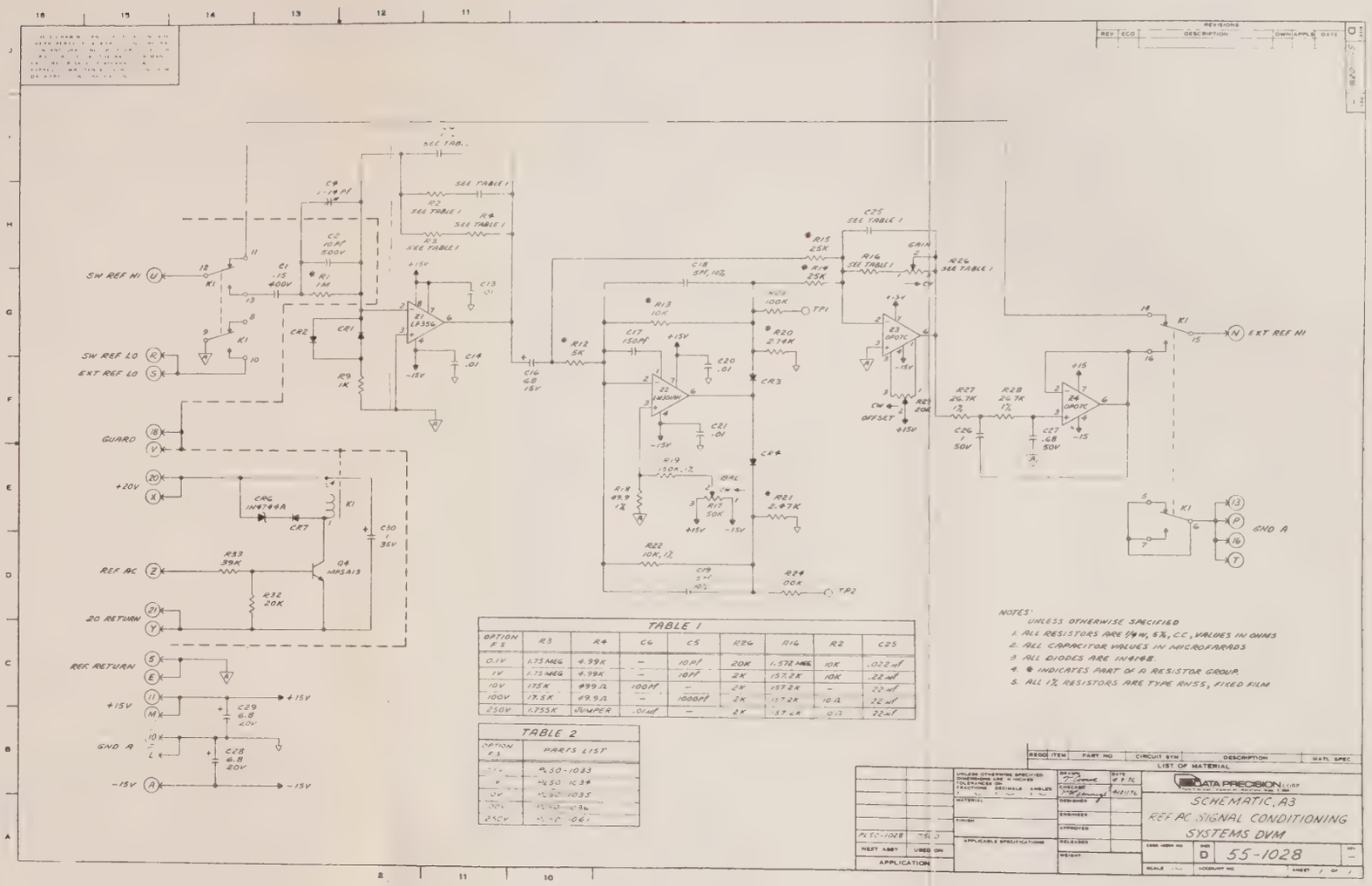


REF. AC SIGNAL CONDITIONING P.C. ASSY (BASIC)
PL50-1028, REV. C

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR,0.15 µf,400V,POLYCARB	23-510025
C2	CAPACITOR,10pf,500V,DM15	23-311001
C4	CAPACITOR,VARIABLE,1-14pf	23-820000
C13,14,20,21	CAPACITOR,.01 µf,CERAMIC	23-111006
C16	CAPACITOR,68 µf,20%,15V,TANT	23-442004
C17	CAPACITOR,150pf,DM15	23-311015
C18,19	CAPACITOR,5pf,10%,DM10	23-310004
C26	CAPACITOR,1 µf,10%,50V,POLYCARB	23-510001
C27	CAPACITOR,0.68 µf,10%,50V,POLYCARB	23-510019
C28,29	CAPACITOR,6.8 µf,20V,TANT	23-441005
C30	CAPACITOR,1 µf,35V,TANT	23-441001
CR1,2,3,4,7	DIODE,SWITCHING,1N4148	24-110001
CR6	DIODE,ZENER,1N4744A	24-121103
K1	RELAY,4 FORM C	25-171004
R9	RESISTOR,1K,¼W,5%,C.C.	22-021029
R12,13	RESISTOR SET,GROUP 9 5K (R12) 10K (R13)	22-58-1012G9
R17	RESISTOR,TRIMMER,50K	22-681009
R18	RESISTOR,FILM,49.9Ω,1%,RN55C	22-3449R9
R19	RESISTOR,FILM,150K,1%,RN55D	22-331503
R20,21	RESISTOR SET,GROUP 18 2740Ω (R20) 2470Ω (R21)	22-58-1012G18
R22	RESISTOR,FILM,10K,1%,RN55C	22-341002
R23,24	RESISTOR,100K,¼W,5%,C.C.	22-021049
R27,28	RESISTOR,FILM,26.7K,1%,RN55C	22-342672
R29	RESISTOR,TRIMMER,20K	22-681008
R32	RESISTOR,20K,¼W,5%,C.C.	22-022039
R33	RESISTOR,39K,¼W,5%,C.C.	22-023939
Q4	TRANSISTOR,MPSA13	24-230A13
Z1	I.C.,OP. AMP,LM356H	24-420356
Z2	I.C., OP. AMP,LM301AH	24-420301
Z3,4	I.C., OP. AMP, OP-07C	24-420007

(SEE PAGE 9-3.1 FOR VARIOUS OPTIONS)



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THE FOLLOWING OPTIONS USE THE BASIC P/L (PL50-1028)
IN ADDITION TO THE FOLLOWING PARTS FOR EACH OPTION

REF. AC SIGNAL CONDITIONING
P.C. ASSY, 0.1V OPTION (01)
PL50-1033, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C5	CAPACITOR,10pf,10%,DM10	23-311001
C25	CAPACITOR,.022 μf,5%,50V	23-510016
R1,3	RESISTOR SET,GR.8 1 MEG (R1) 1.75 MEG (R3)	22-58-1012G8
R2	RESISTOR,10K,¼W,5%,C.C.	22-021039
R4	RESISTOR,FILM,4.99K,1%,RN55C	22-344991
R14,15,16	RESISTOR SET,GROUP 11 25K (R14,15) 1.572 MEG (R16)	22-58-1012G11
R26	RESISTOR,TRIMMER,20K	22-681008

REF. AC SIGNAL CONDITIONING
P.C. ASSY, 1VOPTION (02)
PL50-1034, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C5	CAPACITOR,10pf,10%,DM10	23-311001
C25	CAPACITOR,.22 μf,50V,POLYCARB	23-510017
R1,3	RESISTOR SET,GROUP 8 1 MEG (R1) 1.75 MEG (R3)	22-58-1012G8
R2	RESISTOR,10K,¼W,5%,C.C.	22-021039
R4	RESISTOR,FILM,4.99K,1%,RN55C	22-344991
R14,15,16	RESISTOR SET,GROUP 10 25K (R14,15) 157.2K (R16)	22-58-1012G10
R26	RESISTOR,TRIMMER,2K	22-681005

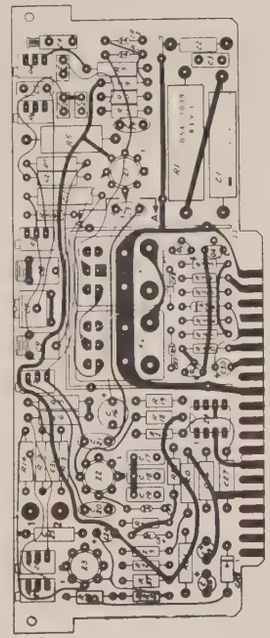
REF. AC SIGNAL CONDITIONING
P.C. ASSY, 10V OPTION (03)
PL50-1035, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C6	CAPACITOR,100pf,5%,DM15	23-311011
C25	CAPACITOR,.22 μf,50V,POLYCARB	23-510017
R1,3	RESISTOR SET, GROUP 8 1 MEG (R1) 175K (R3)	22-58-1012G8
R4	RESISTOR,499Ω,1%,RN55C	22-344990
R14,15,16	RESISTOR SET,GROUP 10 25K (R14,15) 157.2K (R16)	22-58-1012G10
R26	RESISTOR,TRIMMER,2K	22-681005

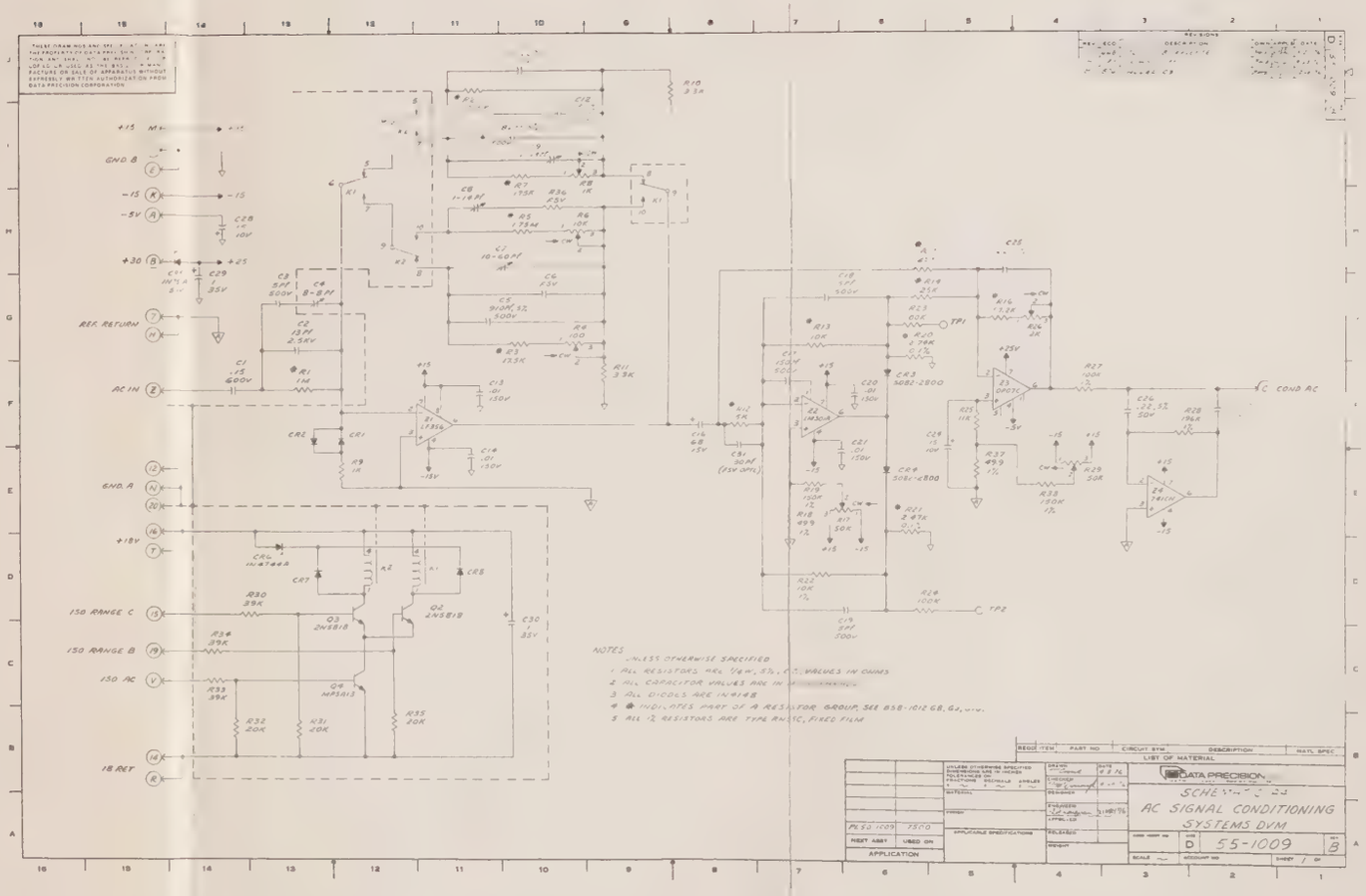
REF. AC SIGNAL CONDITIONING
P.C. ASSY 100V OPTION (04)
PL50-1036, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C5	CAPACITOR,1000pf,5%,DM10	23-311002
C25	CAPACITOR,.22 μf,50V,POLYCARB	23-510017
R1,3	RESISTOR SET,GROUP 8 1 MEG (R1) 17.5K (R3)	22-58-1012G8
R2	RESISTOR,10Ω,¼W,C.C.	22-021009
R4	RESISTOR,49.9Ω,1%,RN55C	22-3449R9
R14,15,16	RESISTOR SET,GROUP 10 25K (R14,15) 157.2K (R16)	22-58-1012G10
R26	RESISTOR,TRIMMER,2K	22-681005

AC SIGNAL CONDITIONING P.C. ASSEMBLY
PL50-1009 REV F



REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, POLYCARB.,0.15 µf,600V	23-510021
C2	GLASS,13pf,2.5KV	23-711001
C3,18,19	MICA,5pf,500V,DM15	23-311000
C4	TRIM.,.8-8pF,GLASS PISTON	23-820001
C5	MICA,910pf,5%,500V,DM15	23-311027
C7	VAR.,10-60pf,CERM	23-810003
C8,9	VAR.,1-14pf,GLASS	23-820000
C10	MICA,82pf,5%,500V,DM10	23-310021
C11	POLYCARB,0.01 µf,2%,50V	23-510024
C12	MICA,5pf,5%,500V,DM10	23-310004
C13,14,20,21	CERM.,.01 µf,150V	23-111006
C16 (Selected for Leakage)	TANT,68 µf,15V MIN	23-442004
C17	MICA,150pf,500V,DM15	23-311015
C24,28	TANT,15 µf,20%,10V	23-441003
C25,26,27	POLYCARB,0.22 µf,5%,50V	23-510017
C29,30	CAPACITOR,TANT,1 µf,35V	23-441001
C31	CAPACITOR,MICA,30pf,500V,DM15	23-311005
CR1,2,7,8	DIODE,SWITCH 1N4148	24-110001
CR6	DIODE,ZENER 1N4744A	24-121103
CR5	DIODE,ZENER 1N751A	24-120073
CR3,4	DIODE,SWITCH 5082-2800	24-110004
K1,2	RELAY, 2 FORM C	25-171002
Q2,3	TRANSISTOR,NPN, 2N5818	24-235818
Q4	TRANSISTOR,DARLINGTON,MPSA13	24-230A13
R1,2,3,5,7	RESISTOR SET, GROUP 8	22-58-1012G8
	1 MEG (R1)	
	1.755K (R2)	
	17.5K (R3)	
	175K (R7)	
	1.75 MEG (R5)	
R9	RESISTOR,1K,¼W,5%,C.C.	22-021029
R10,11	3.3K,¼W,5%,C.C.	22-023329
R18,37	FILM,49.9Ω,1%,RN55C	22-3449R9
R19,38	RESISTOR,FILM,150K,1%,RN55D	22-331503
R20,21	RESISTOR SET, GROUP 18	22-58-1012G18
	2740Ω (R20)	
	2470Ω (R21)	
R22	RESISTOR,FILM,10K,1%,RN55C	22-341002
R12,13	RESISTOR SET, GROUP 9	22-58-1012G9
	10K (R13)	
	5K (R12)	
R14,15,16	RESISTOR SET, GROUP 10	22-58-1012G10
	157.2K (R16)	
	25K (R14,R15)	
R25	RESISTOR,11K,¼W,5%,C.C.	22-021139
R27	FILM,100K,1%,RN55C	22-341003
R28	FILM,196K,1%,RN55C	22-341963
R30,33,34	39K,¼W,5%,C.C.	22-023939
R31,32,35	20K,¼W,5%,C.C.	22-022039
R23,24	100K,¼W,5%,C.C.	22-021049
R4	TRIMMER, 100Ω	22-681002
R6	TRIMMER, 10K	22-681007
R8	TRIMMER, 1K	22-681004
R17,29	TRIMMER, 50K	22-681009
R26	RESISTOR,TRIMMER, 2K	22-681005
Z1	I.C., OP. AMP., LF356	24-420356
Z2	I.C., OP. AMP., LM301A	24-420301
Z3	I.C., OP. AMP., OPO7C	24-420007
Z4	I.C., OP. AMP., 741CN	24-400741


AC SIGNAL CONDITIONING
SYSTEMS DVM
55-1009
NOTES
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W, 5%, C.C. VALUES IN OHMS
2. ALL CAPACITOR VALUES ARE IN
3. ALL DIODES ARE IN4148
4. # INDICATES PART OF A RESISTOR GROUP. SEE B58-1012 GB, G2, ...
5. ALL 1% RESISTORS ARE TYPE RN55C, FIXED FILM

9-4

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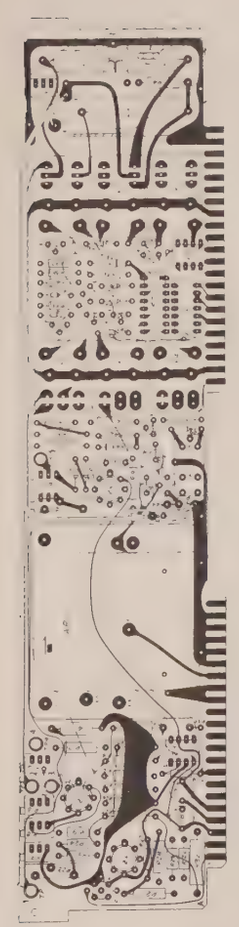
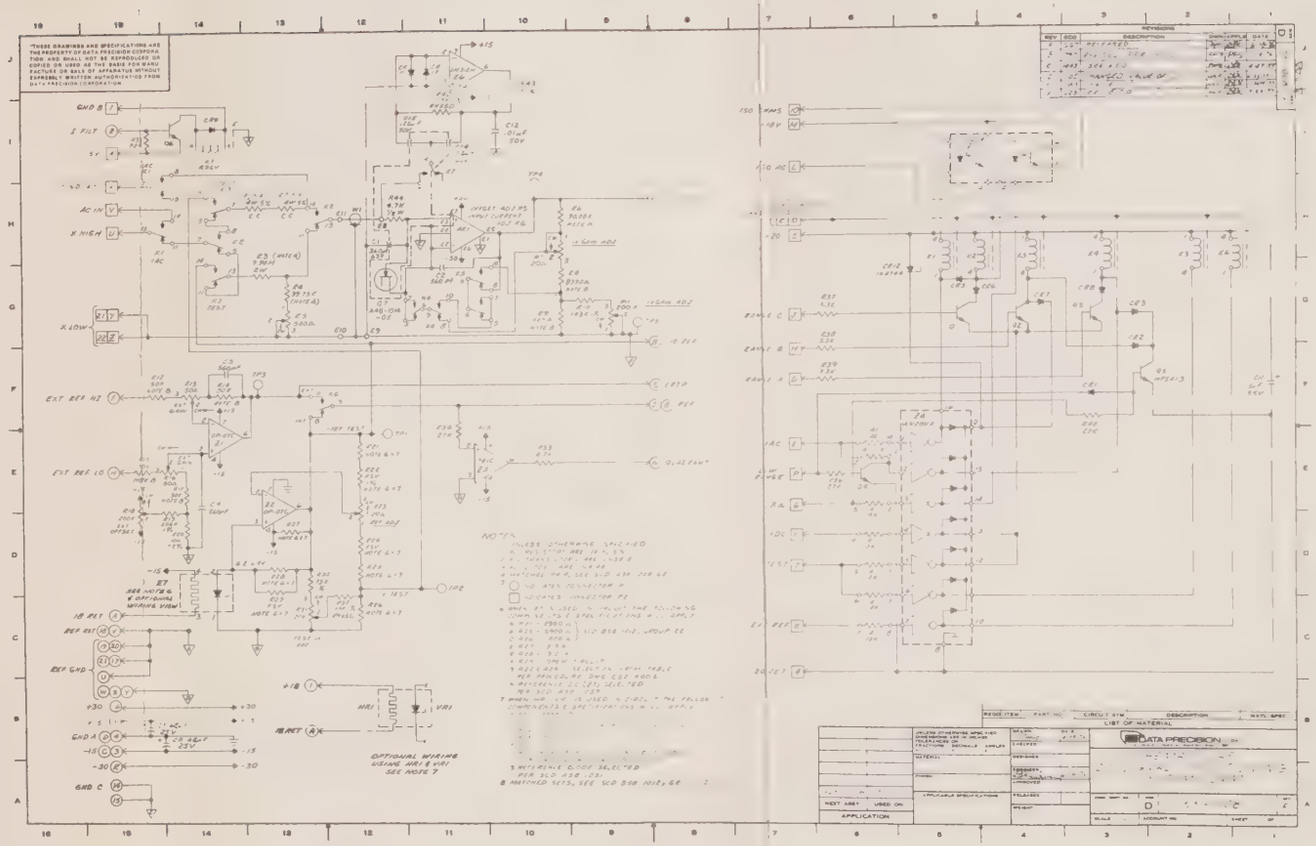
D.C. SIGNAL CONDITIONING P.C. ASSEMBLY
PL50-1008 REV J



REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A1	RESISTOR NETWORK,10K,DIP	22-701003
AR1	AMPLIFIER ASSY (D57-1032)	PL50-1032
C1	CAPACITOR,360pf,5%,63V,POLYSTY	23-550110
C2,3,4	CAPACITOR,560pF,5%,160V,POLYSTY	23-550106
C7,8	CAPACITOR,68uf,25V	23-442005
C11	CAPACITOR, 1uf,35V,TANT	23-441001
C12	CAPACITOR, 0.01uf,50V,DISC	23-118002
C14,15	CAPACITOR, 0.22uf,50V,PC	23-510017
CR1,2,3,5 thru 11	DIODE,SWITCHING, 1N4148	24-110001
CR12	DIODE,ZENER, 1N4744A,15V	24-121103
K1,2,3	RELAY, 2 FORM C, 2KV	B58-1014
K4,5,6	RELAY, 2 FORM C	25-171002
K7	RELAY, RS6V	25-170010
Q1,2,3,4,6	TRANSISTOR, NPN, 2N5818	24-235818
Q5	TRANSISTOR, NPN, MPS-A13	24-230A13
Q7	TRANSISTOR,FET,YEL. DOT	24-48-1014-05
R1,2	RESISTOR, 51K, 4W, 5%	22-065139-C
R3,R4	RESISTOR SET, GROUP 2 9.90 MEG, 2W (R3) 99.75K (R4)	22-38-1002G2
R5	RESISTOR,TRIM,500Ω	22-681003
R13,16	RESISTOR, TRIM, 50Ω	22-681001
R11,18	RESISTOR, TRIM, 200K	22-681010
R7,23	RESISTOR, TRIM, 20Ω	22-681100
R6,8,9	RESISTOR SET, GROUP 2 90.00K (R6) 8990Ω (R8) 1005Ω (R9)	22-58-1012G2
R10	RESISTOR,143K,1%,RN55D,FILM	22-331433
R12,14,15,17	RESISTOR SET, GROUP 3 50K (R12,14,15,17)	22-58-1012G3
R20	RESISTOR,SEMI PRECISION,10Ω,2%	22-121000
R21,25,26	RESISTOR SET, GROUP 22 2900Ω (R21) 5800Ω (R25) 1000Ω (R26)	22-58-1012G22
R27	RESISTOR,3.9K,¼W,5%,C.C.	22-023929
R28	RESISTOR,3.01K,1%,RN55D	22-333011
R31	RESISTOR, TRIM, 20K	22-681008
R19,42	RESISTOR,205K,1%,RN55D	22-332053
R30	RESISTOR,75K,1%,RN55C	22-347502
R32	RESISTOR,1 MEG,1%,RN65C	22-392001
R22,24	RESISTOR SET,FILM,FSV,1%,RN55	22-52-4002
R33	RESISTOR,4.7K,¼W,5%,C.C.	22-024729
R37,38,39	RESISTOR,3.3K,¼W,5%,C.C.	22-023329
R35	RESISTOR,22K,¼W,5%,C.C.	22-022239
R34,36,40	RESISTOR,27K,¼W,5%,C.C.	22-022739
R43	RESISTOR,51Ω,¼W,5%	22-025109
R44	RESISTOR,4.7K,½W,C.C.	22-034729-C
Z1,2	I.C., OP. AMP, OP-07C	24-420007
Z3	I.C., OP. AMP, 741C	24-400741
Z5	I.C. OPTOISOLATOR, ILD74	24-NILD74
Z4	I.C., HV BUFFER, ULN2001A	24-330000
Z6	I.C., OP-05	24-420005
Z7	SELECTED PREC. REF. I.C. (LM299)	24-58-1059



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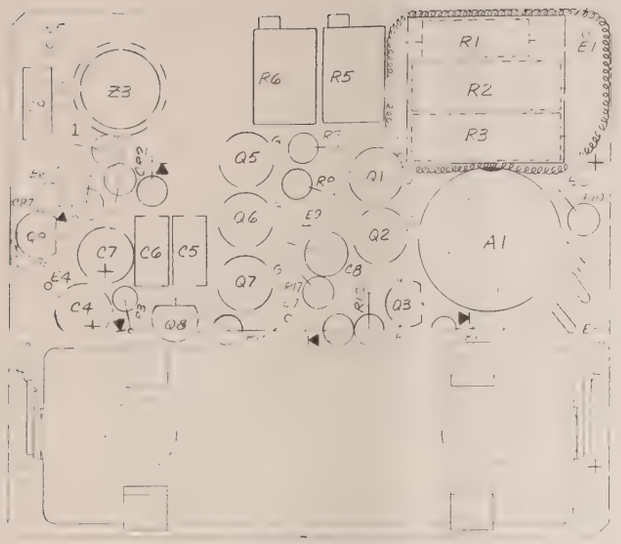
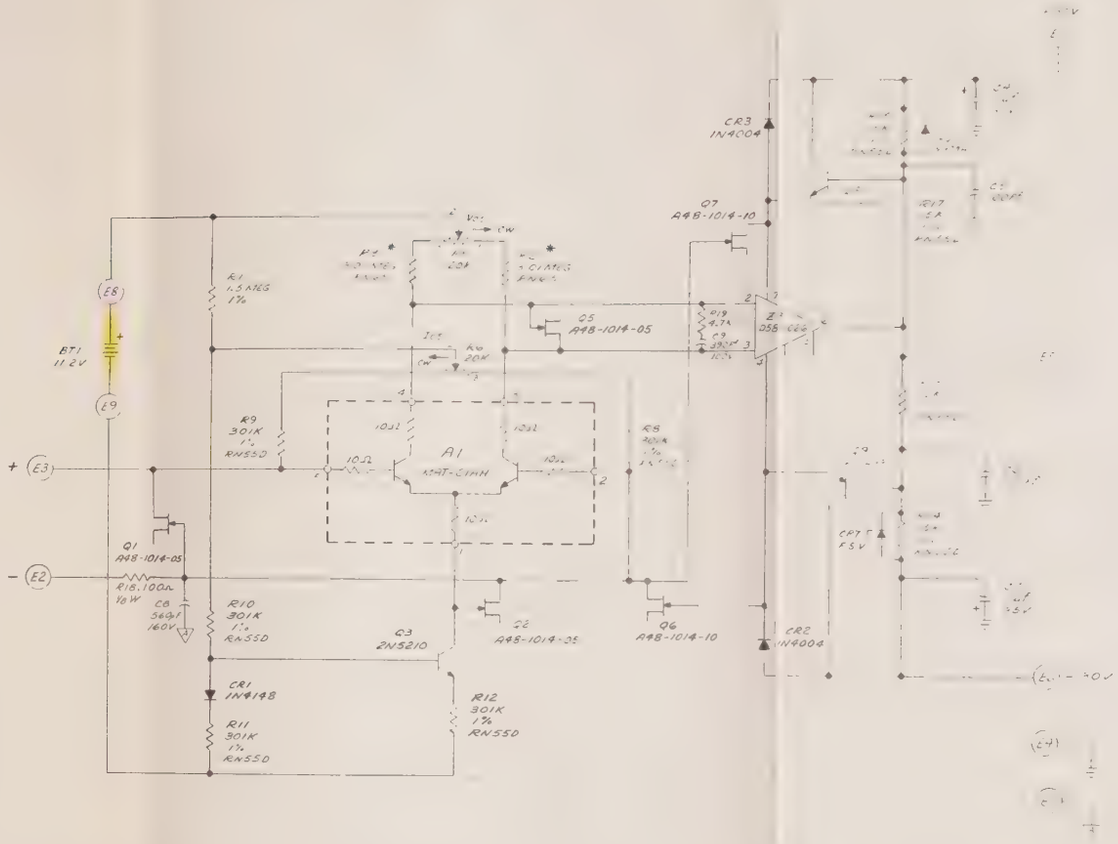


INPUT AMPLIFIER P.C. ASSEMBLY
PL50-1031, REV. D

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A1	TRANSISTOR ASSY (BS7-1030)	PL50-1030
BT1	BATTERY,MERCURY	B58-1036
C4,7	CAPACITOR,1μf,35V	23-441001
C5,6	CAPACITOR,100pf,DM10	23-310023
C8	CAPACITOR,560pf,160V	23-550106
C9	CAPACITOR,390pf,DM10	23-310037
CR1	DIODE,SWITCHING,1N4148	24-110001
CR2,3	DIODE, 1N4004	24-104004
CR6	DIODE, 1N970A	24-120114
Q1,2,5	TRANSISTOR,FET,YEL. DOT	24-48-1014-05
Q3	TRANSISTOR,2N5210	24-235210
Q6,7	TRANSISTOR,FET,ORN DOT	24-48-1014-10
Q8	TRANSISTOR,MPS-A42	24-230A42
Q9	TRANSISTOR,MPS-A93	24-240A93
R1	RESISTOR,1.5MEG,1%	22-470000
R2,3	RESISTOR,3.01 MEG	22-58-1027
R5,6	RESISTOR,TRIMMER,20K	22-681008
R8,9,10,11,12	RESISTOR,301K,1%,RN55D	22-333013
R13,14,15,17	RESISTOR,15K,1%,RN55D	22-331502
R18	RESISTOR,100Ω,1/8W,5%	22-011019
R19	RESISTOR,4.7K,¼W,5%	22-024729



NOTES:
1. * INDICATES RESISTORS MATCHED TO ± .1% TC TRACKING TO 10 PPM/°C, SEE SCD B58-1027.

RECD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC
				LIST OF MATERIAL	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN T. Cowan DATE 3/11/76
MATERIAL	CHECKED [illegible] 4-19-76
FINISH	DES OWNER
	ENGINEER [illegible] 4-16-76
	APPROVED
APPLICABLE SPECIFICATIONS	RELEASED
	WEIGHT
NEXT ASSY USED ON	
APPLICATION	

DATA PRECISION IND

SCHEMATIC, ASARI
INPUT AMPLIFIER
SYSTEMS DVM

CODE IDENT NO	SIZE	55-1017	REV
	D		D
SCALE	ACCOUNT NO	SHEET 1 OF 1	

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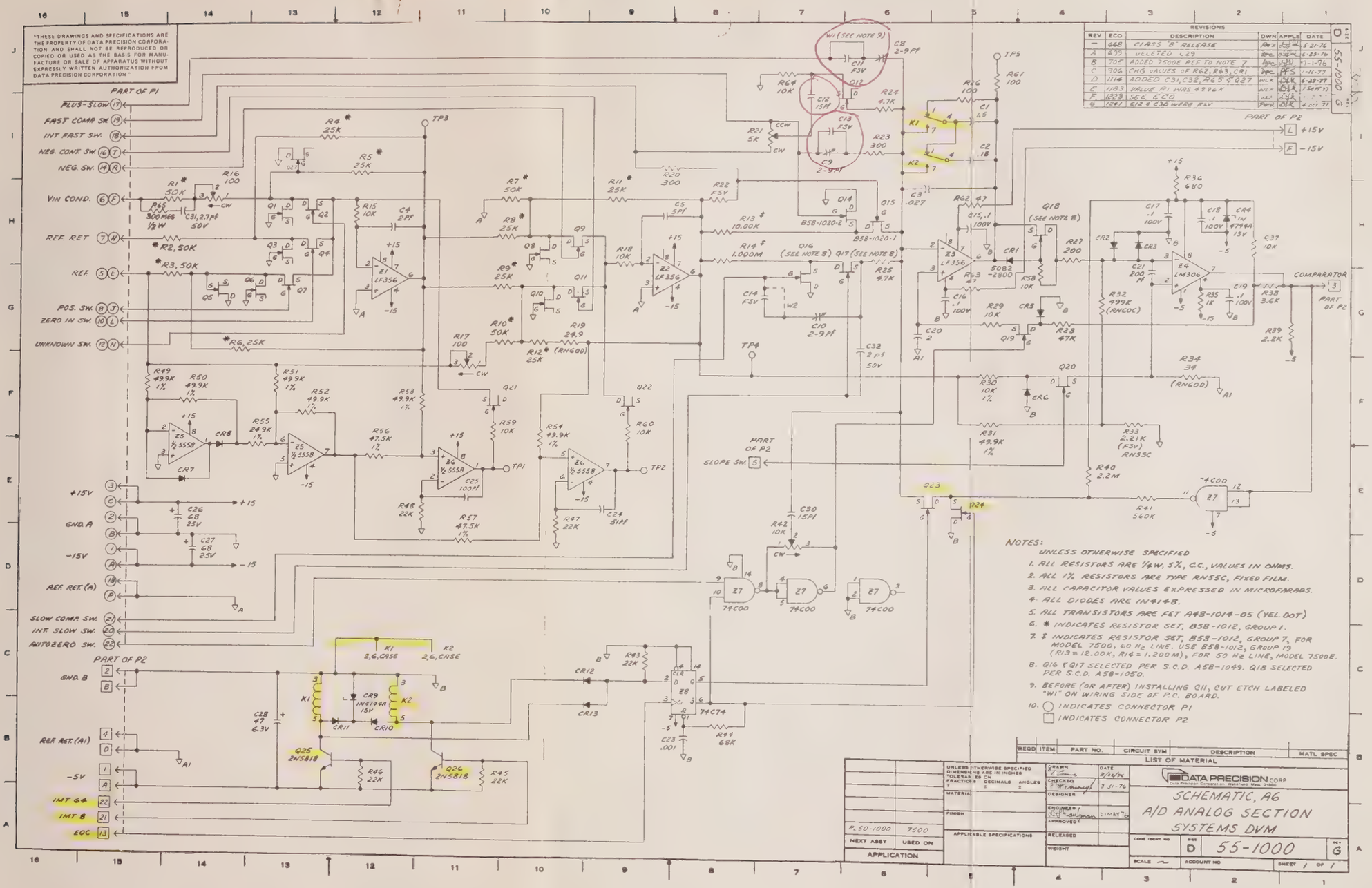

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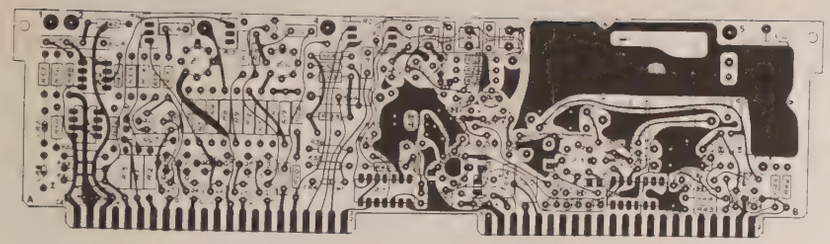
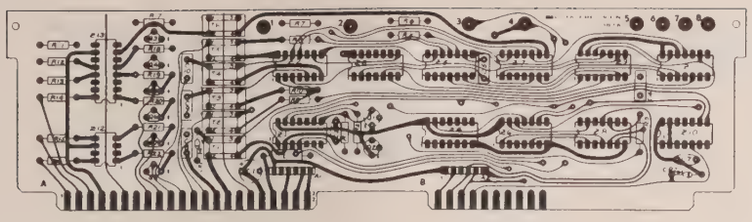


A/D ANALOG SECT. P.C. ASSY
PL50-1000 REV. L

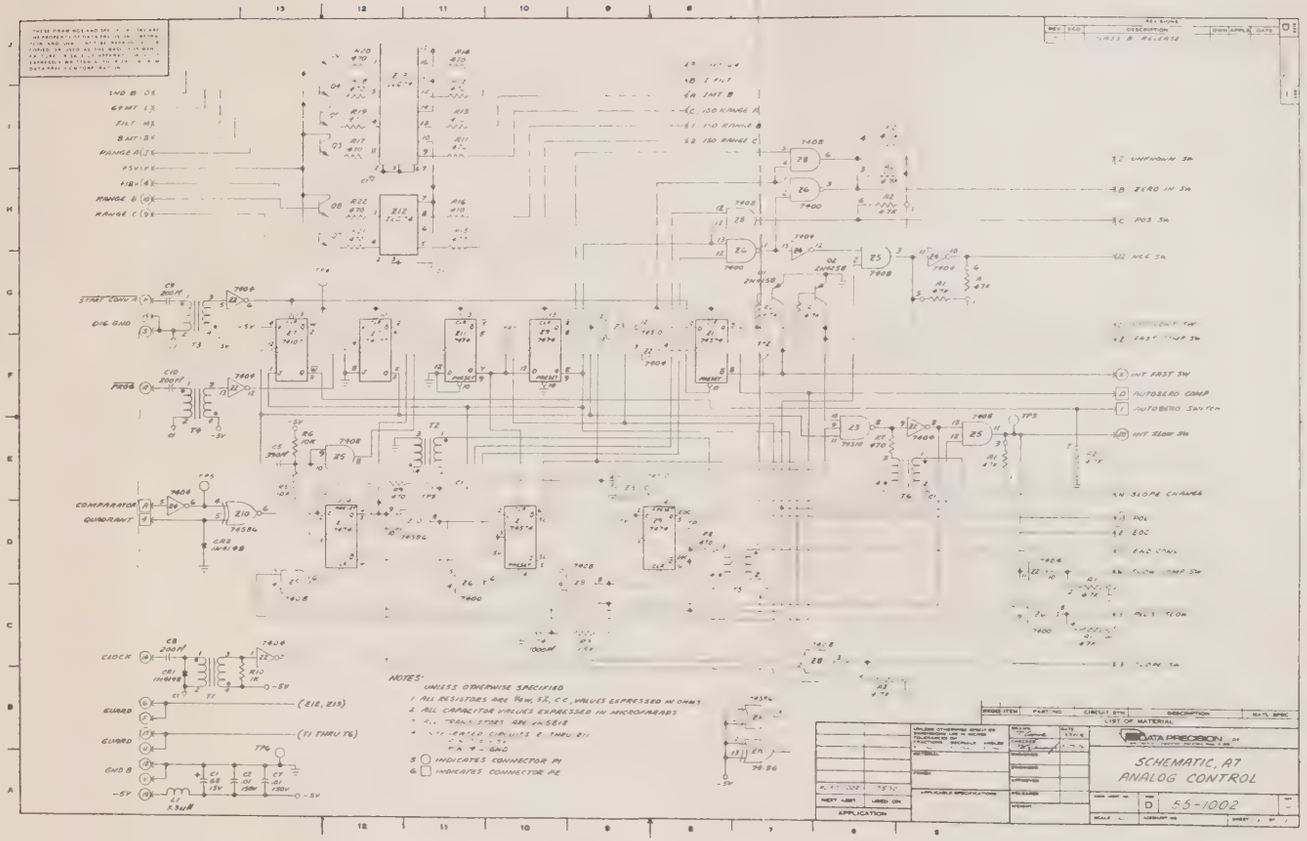
REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1,2,3	CAPACITOR SET	23-58-1022
	1.5 µf (C1)	
	0.18 µf (C2)	
	0.027 µf (C3)	
C4	CAPACITOR, 2 pf, DM15 (or DM10)	23-311004
C5	5 pf, DM15 (or DM10)	23-310004
C8,9,10	Var. 2-9 pf	23-810006
C15,16,17,18,19	0.1 µf, 100V	23-141001
C20	2 µf, 10%, 50V	23-510002
C21	CAPACITOR, 200 pf, DM15	23-311018
C23	CAPACITOR, 0.001 µf, 20% DISC	23-118202
C24	51 pf, DM15	23-311006
C25	100 pf	23-311011
C26,27	68 µf, 25V	23-441053
C28	CAPACITOR, 47 µf, 6.3V	23-441053
C12,30	CAPACITOR, 15pf, DM15 (FSV)	23-311003
C31	CAPACITOR, 2.7pf, 50V	23-110002
C32	CAPACITOR, 2pf, 50V	23-310001
CR1	DIODE, SCHOTTKY, 5082-2800	24-110004
CR2,3,5,6,7,8 CR10,11,12,13	DIODE 1N4148	24-110001
CR4,9	DIODE 1N4744A	24-121103
K1,K2	RELAY, RS-6V	S425-170010
Q1,2,3,4,5,6,7,8,9 Q10,11,12,19,20,21 Q22,23,24,27	TRANSISTOR, FET, YELLOW DOT	24-48-1014-05
Q15	TRANSISTOR, FET	24-58-1020-1
Q14	TRANSISTOR, FET	24-58-1020-2
Q17	TRANSISTOR PAIR, N CHANNEL JFET	24-58-1049-1
Q18	TRANSISTOR, FET, SELECTED	24-58-1050
Q16	TRANSISTOR PAIR, N CHANNEL JFET	24-58-1049-2
Q25,26	TRANSISTOR, 2N5818	24-235818
R1 Thru R12	RESISTOR SET, GROUP 1	22-58-1012G1
	50K (R1,2,3,7,10)	
	25K (R4,5,6,8,9,11,12)	
R13,14	RESISTOR SET, GROUP 7	22-58-1012G7
	10.00K (R13)	
	1.000K (R14)	
R19	RESISTOR, 24.9Ω, RN60D	22-3624R9
R30	10K, RN55C	22-341002
R31,49,50,51,52,53,54	49.9K, RN55C	22-344992
R33	2.21K (FSV), RN55C	
R34	34Ω, RN60D	22-3634R0
R32	499K, RN60C	22-374993
R55	24.9K, RN55C	22-342492
R56,57	RESISTOR, 47.5K, RN55C	22-344752
R16,17	RESISTOR, TRIM, 100Ω	22-681002
R21	RESISTOR, TRIM, 5K	22-681006
R42	RESISTOR, TRIM, 10K	22-681007
R15,18,29,37,58,59 R60,64	RESISTOR, 10K, ¼W, 5%, C.C.	22-021039
R20,23	300Ω	22-023019
R24,25	4.7K	22-024729
R26,61	100Ω	22-021019
R27	200Ω	22-022019
R28	47K	22-024739
R35	1K	22-021029
R36	680Ω	22-026819
R38	3.6K	22-023629
R39	2.2K	22-022229
R40	2.2MEG	22-022259
R41	560K	22-025649
R43,45,46,47,48	22K	22-022239
R44	RESISTOR, 68K, ¼W, 5%, C.C.	22-026839
R62,63	RESISTOR, 47Ω, ¼W, 5%, C.C.	22-024709
R65	RESISTOR, 300MEG, ½W, C.C.	22-033077
Z1,2,3	I.C. LF356H	24-420356
Z4	I.C. LM306H	24-420306
Z5,6	I.C. 5558	24-405558
Z7	I.C. 74COON	24-G74COO
Z8	I.C. 74C74N	24-G74C74

25-170010 $20.40 9/6/85



ANALOG CONTROL P.C. ASSY
PL50-1002, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A1,2	RESISTOR NETWORK, 4.7K	22-58-1003-2
C1	CAPACITOR,68 µf,15V MIN.	23-442004
C2,C7	0.01 µf,150V,DISC	23-111006
C4	1000pf,DM10	23-311002
C5	390pf,DM15	23-311026
C8,9,10	CAPACITOR,200pf,DM15	23-311018
CR1,2	DIODE IN4148	24-110001
L1	INDUCTOR, 3.3 mH	25-100003
Q1,2	TRANSISTOR 2N4258	24-244258
Q3,4,5,6,7,8	TRANSISTOR 2N5818	24-235818
R1,2	RESISTOR,4.7K,¼W,5%,C.C.	22-024729
R3	1.5K,	22-021529
R5,6	10K,	22-021039
R7,8,9,11,12,13,14	470Ω	22-024719
R15,16,17,18,19,20		
R21,22		
R10	RESISTOR, 1K, ¼W,5%,C.C.	22-021029
T1	TRANSFORMER ASSY	C58-1006
T2,3,4,5,6	TRANSFORMER ASSY	C58-1011
Z1	I.C. SN74S74N	24-E74S74
Z2,4	I.C. SN7404N	24-A07404
Z3	I.C. SN74S10N	24-E74S10
Z5,8	I.C. SN7408N	24-A07408
Z6	I.C. SN7400N	24-A07400
Z7	I.C. SN74107N	24-A74107
Z9,11	I.C. SN7474N	24-A07474
Z10	I.C. SN74S86N	24-E74S86
Z12	I.C. ILD74	24-NILD74
Z13	I.C. ILQ74	24-NILQ74



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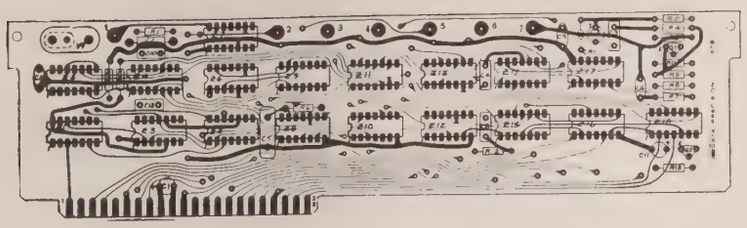
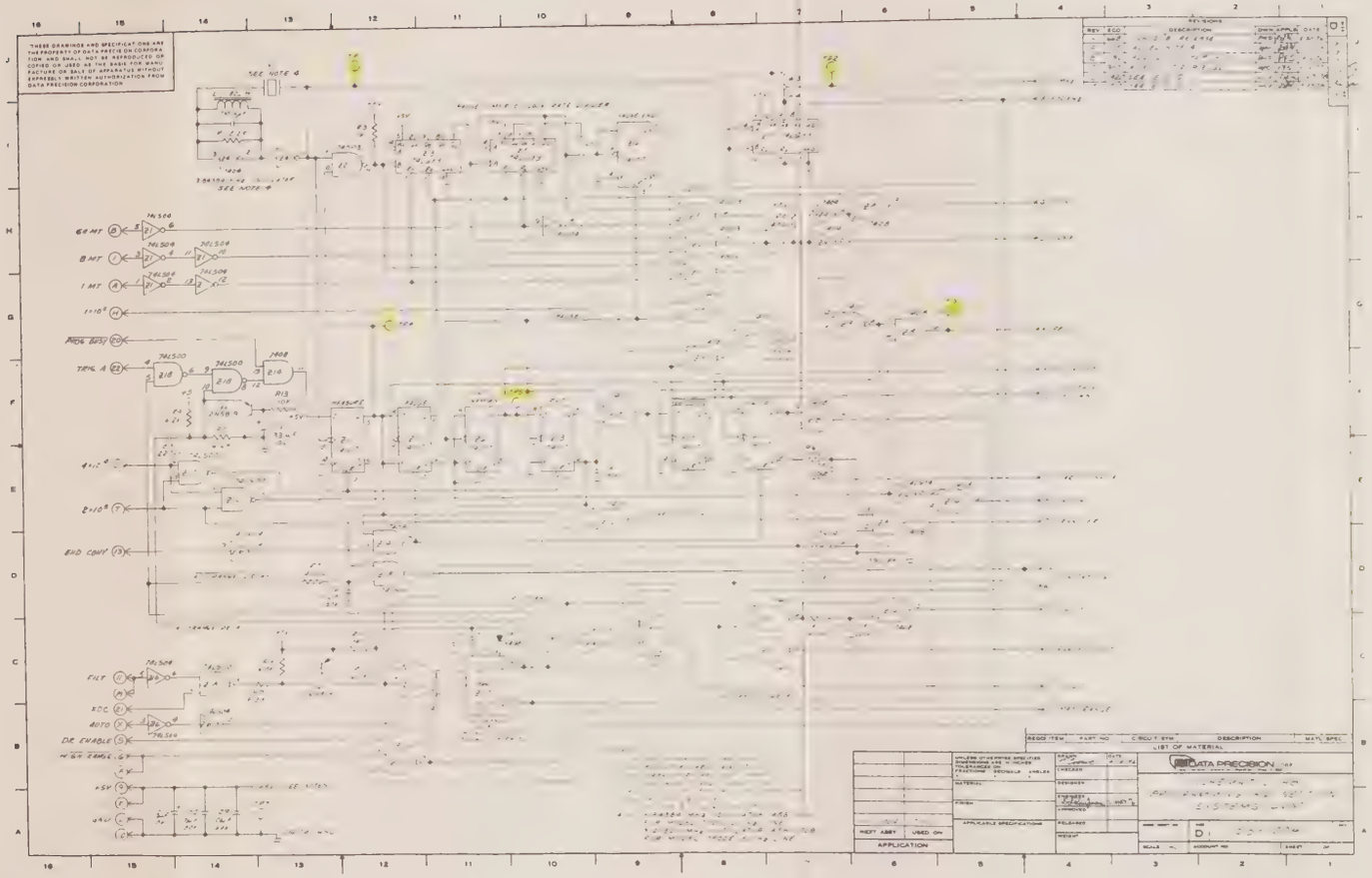


PROGRAMMING A/D SECTION P.C. ASSY
PL50-1004, REV. F

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR,15 µf,10V	23-441003
C2,6,9	0.01 µf,150V,DM15	23-111006
C3,8	220 pf, DM15	23-311020
C4,12	390 pf, DM15	23-311026
C5	0.0068 µf, 100V, 10%	23-210309
C7,11	CAPACITOR, 33µf,10V,10%	23-441004
C10	CAPACITOR,5pf,500V,5%	23-311000
CR1	DIODE 1N4148	24-110001
L1	INDUCTOR 180 uH	25-100026
Q1,2	TRANSISTOR, 2N5819	24-245819
R1	RESISTOR, 2.2K, ¼W, 5%	22-022229
R2,7,12	470Ω,	22-024719
R3	1K,	22-021029
R4,5,8,9,11	6.2K,	22-026229
R6	100Ω,	22-021019
R10	RESISTOR, 36K, ¼W, 5%	22-023639
R13	RESISTOR, 100K, ¼W, 5%	22-021049
Z1,16	I.C. 74LS04	24-E0LS04
Z2	I.C. 74S03	24-F74S03
Z3,5,7	I.C. 74LS93N	24-E0LS93
Z4	I.C. 7404N	24-A07404
Z6,11,13,15	I.C. 74107N	24-A74107
Z8,14	I.C. 7408N	24-A07408
Z9,12	I.C. 7400N	24-A07400
Z10,18	I.C. 74LS00	24-E0LS00
Z17	I.C. U6A960159	24-A09601
Y1	CRYSTAL 3.84384 MC	A58-1010



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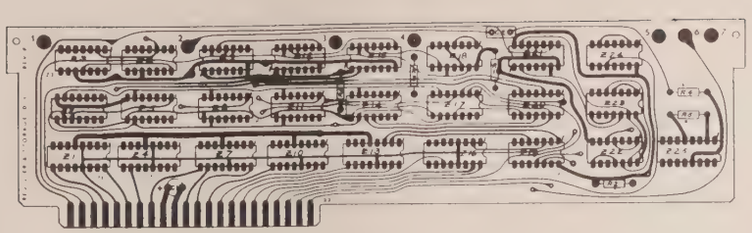
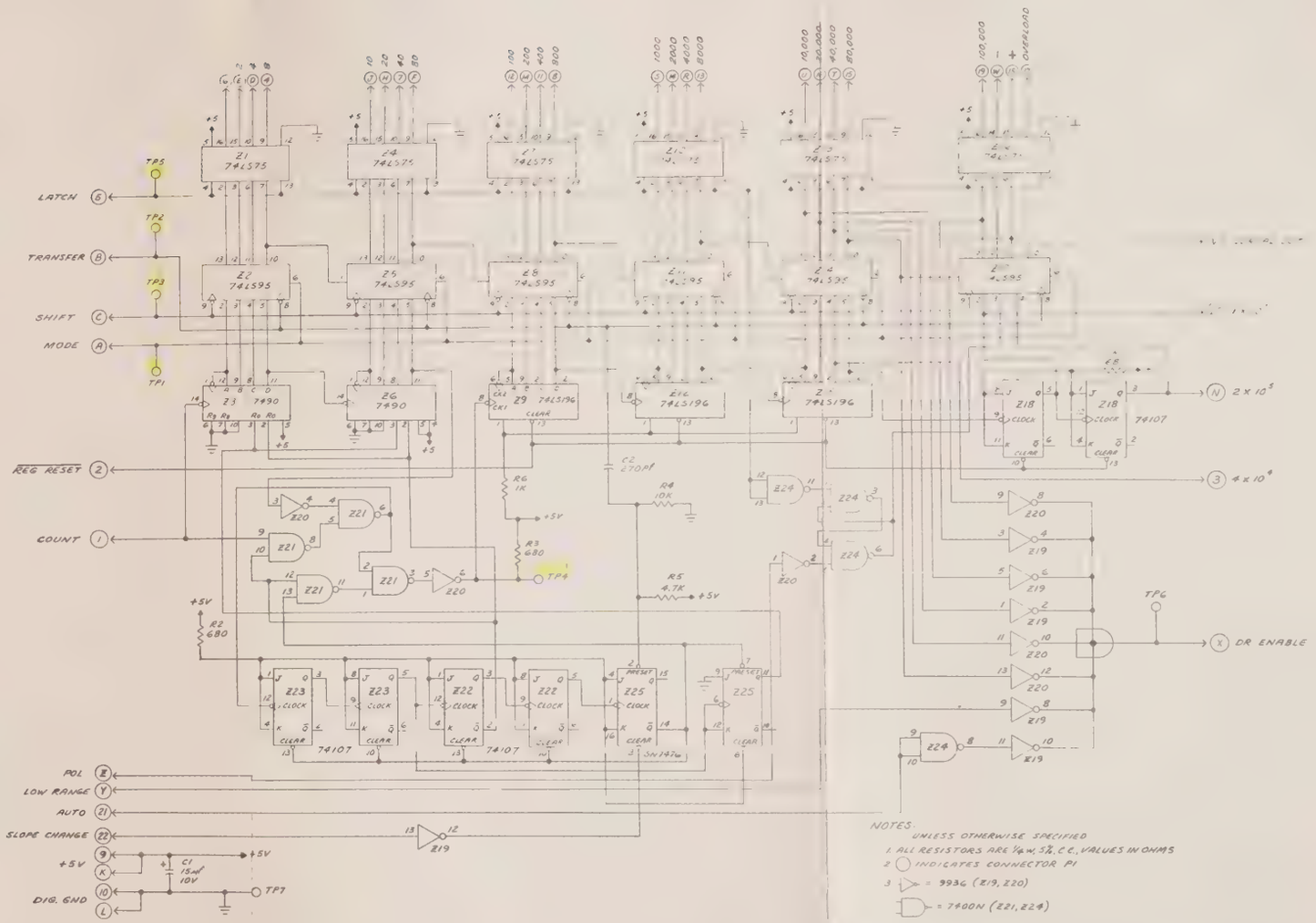


REGISTER & STORAGE P.C. ASSY
PL50-1003, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 15 µf, 10V	23-441003
C2	CAPACITOR, 270 pf, DM15	23-311022
R1,2,3	RESISTOR, 680Ω, ¼W, 5%, C.C.	22-026819
R4	RESISTOR, 10K, ¼W, 5%, C.C.	22-021039
R5	RESISTOR, 4.7K, ¼W, 5%, C.C.	22-024729
R6	RESISTOR, 1K, ¼W, 5%, C.C.	22-021029
Z1,4,7,10,13,16	I.C. SN74LS75N	24-E0LS75
Z2,5,8,11,14,17	I.C. SN74LS95N	24-E0LS95
Z3,6	I.C. SN7490N	24-A07490
Z9,12,15	I.C. SN74LS196N	24-E0LS196
Z18,22,23	I.C. SN74107N	24-A74107
Z19,20	I.C. 9936	24-469936
Z21,24	I.C. SN7400N	24-A07400
Z25	I.C. SN7476N	24-A07476



I C	GND	+5
Z2, 5, 8, 9, 11, 12, 14, 15, 17, 18, 19, 20, 21, 22, 23, 24	PIN 7	PIN 14
Z1, 4, 7, 10, 13, 16	PIN 12	PIN 5
Z3, 6	PIN 10	PIN 5
Z25	PIN 13	PIN 5

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

DRAWN CHECKED DESIGNER ENGINEER APPROVED RELEASED WEIGHT

DATE

DATA PRECISION CORP

SCHEMATIC, A9
REGISTER & STORAGE
SYSTEMS DVM

PL50-1003	7500
NEXT ASSY	USED ON
APPLICATION	

SIZE D | 55-1003 | REV B

SCALE | ACCOUNT NO | SHEET 1 OF 1

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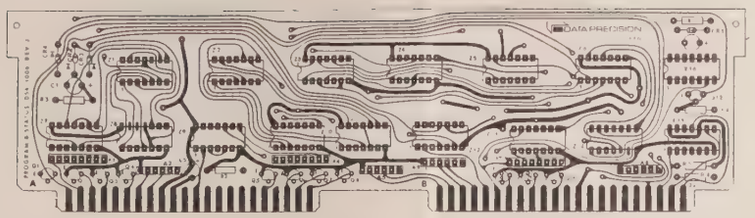
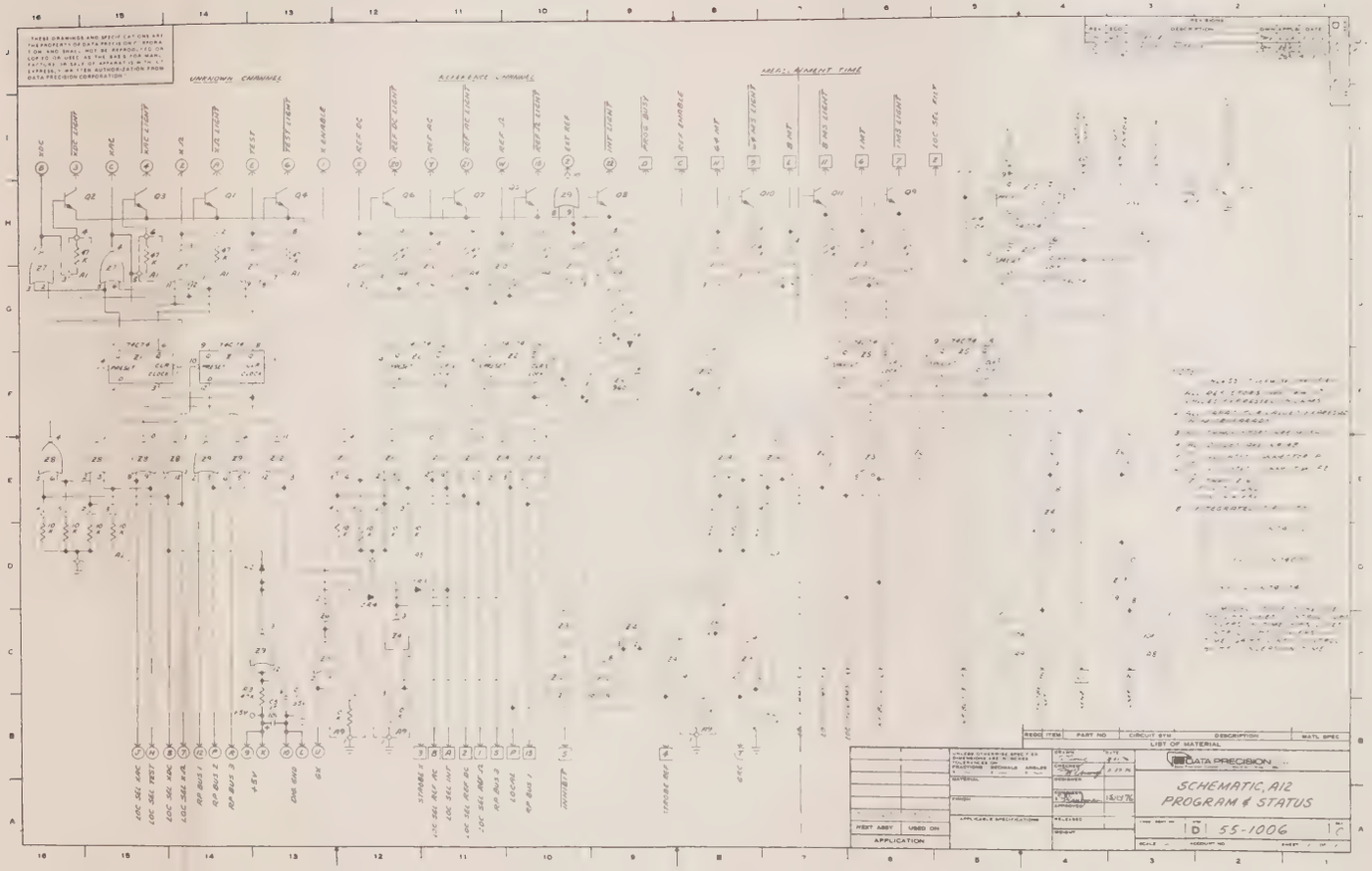


PROGRAM & STATUS P.C. ASSY
PL50-1006, REV. B

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A1,4,7	RESISTOR NETWORK, 47K	22-58-1000-1
A2,5,8,9	RESISTOR NETWORK, 10K	22-58-1003-1
C1	CAPACITOR, 1 µf, 35V	23-441001
C2,5	CAPACITOR, 15 µf, 10V	23-441003
CR1,2,3,4	DIODE 1N4148	24-110001
Q1 thru Q12	TRANSISTOR MPS-A13	24-230A13
R1,2,4,5	RESISTOR, 10K, ¼W, 5%, C.C.	22-021039
R3,6	RESISTOR, 47K, ¼W, 5%, C.C.	22-024739
Z1,2,5,15	I.C. MM74C74N	24-G74C74
Z3,7,8,9,10,11,13,14	I.C. MM74C02N	24-G74C02
Z4,12	I.C. MM74C00N	24-G74C00
Z6	I.C. MM74C04N	24-G74C04
Z16	I.C. U6A960159	24-A09601



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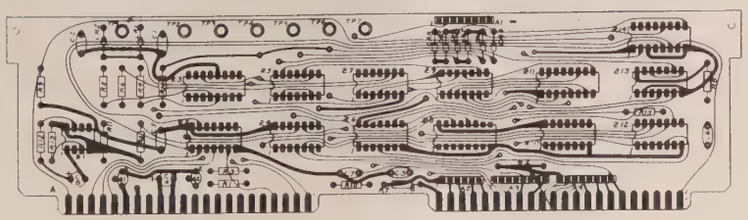
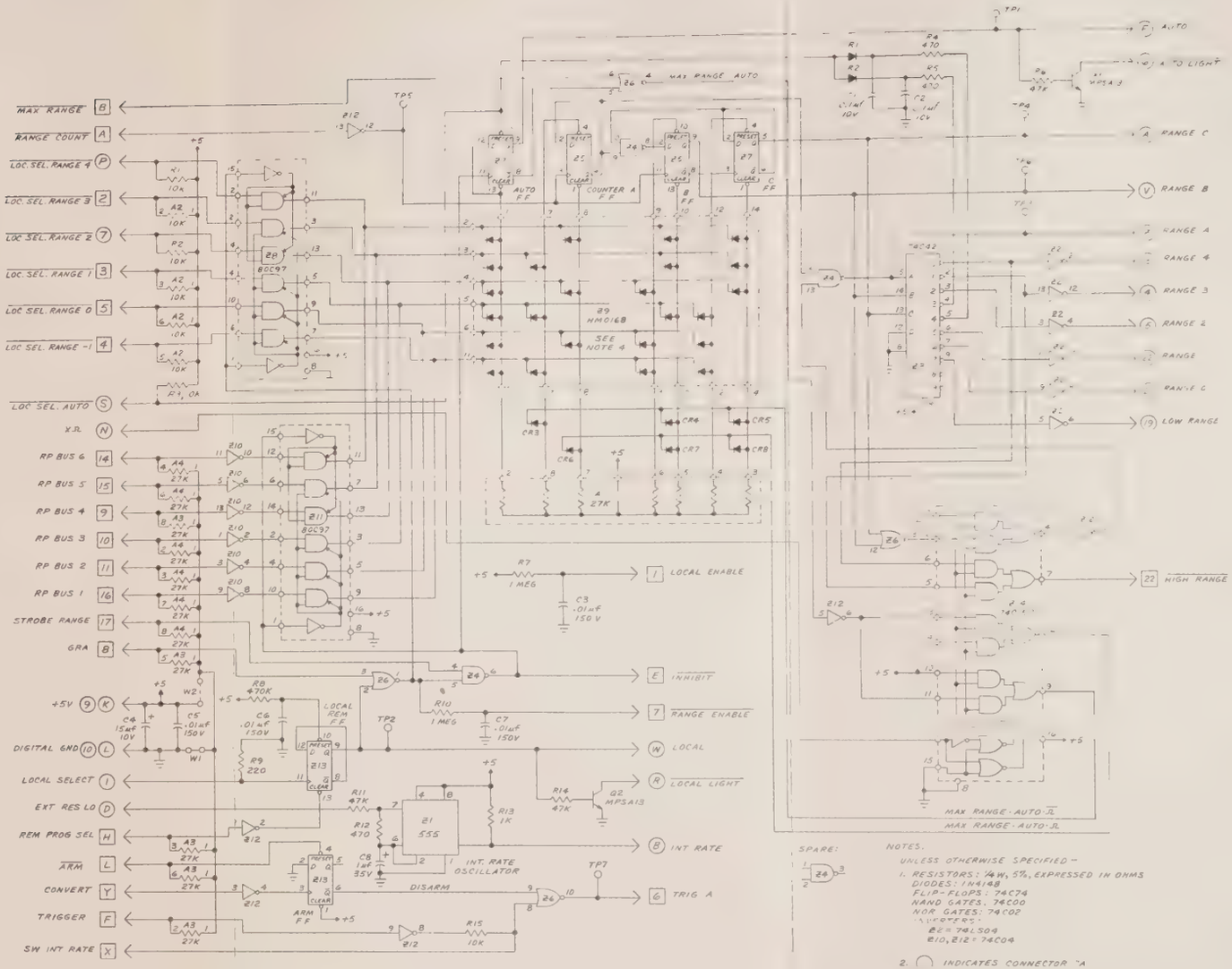


RANGE MODULE P.C. ASSY
PL50-1007 REV. B

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A1,3,4	RESISTOR NETWORK,8 PIN SIP,27K	22-730003
A2	RESISTOR NETWORK, 6 PIN SIP,10K	22-58-1003-1
C1,2	CAPACITOR, 0.1 µf, 10V	23-118206
C3,5,6,7	CAPACITOR, 0.01 f, 150V	23-111006
C4	CAPACITOR, 15 µf, 10V	23-441003
C8	CAPACITOR, 1 µf, 35V	23-441001
CR1 thru CR8	DIODE 1N4148	24-110001
Q1,2	TRANSISTOR, MPS-A13	24-230A13
R1,2,3,15	RESISTOR, 10K, ¼W, 5%	22-021039
R4,5,12	470Ω,	22-024719
R6,11,14	47K,	22-024739
R7,10	1 MEG,	22-021059
R8	470K,	22-024749
R9	220Ω,	22-022219
R13	RESISTOR, 1K, ¼W, 5%	22-021029
Z1	I.C. NE555V	24-400555
Z2	I.C. 74LS04	24-E0LS04
Z3	I.C. MM74C42N	24-G74C42
Z4	I.C. MM74C00N	24-G74C00
Z5,7,13	I.C. MM74C74N	24-G74C74
Z6	I.C. MM74C02N	24-G74C02
Z8,11	I.C. MM80C97N	24-G80C97
Z9	DIODE MATRIX	C58-1052
Z10,12	I.C. MM74C04N	24-G74C04
Z14	I. C. MM74C157N	24-G74C157



NOTES.
UNLESS OTHERWISE SPECIFIED -
1. RESISTORS: ¼W, 5%, EXPRESSED IN OHMS
DIODES: 1N4148
FLIP-FLOPS: 74C74
NAND GATES: 74C00
NOR GATES: 74C02
INVERTERS:
Z2 = 74LS04
Z10, Z12 = 74C04
2. ◠ INDICATES CONNECTOR "A"
▭ INDICATES CONNECTOR "B"
3. GND = PIN 7, +5 = PIN 14 ON: Z2, Z4, Z5, Z6, Z7, Z10, Z12, & Z13
4. Z9 PROGRAMMED PER SPEC CONTROL DWG C58-1052

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC
LIST OF MATERIAL					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
NEXT ASSY USED ON
APPLICATION

DRAWN DATE 3 MAY 76
CHECKED
DESIGNER
ENGINEER 14 MAY 76
APPROVED
RELEASED
WEIGHT

DATA PRECISION CORP

SCHEMATIC, A13
RANGE MODULE
SYSTEMS DVM

CODE IDENT NO SIZE D 55-1007 REV B
SCALE ACCOUNT NO SHEET 1 OF 1

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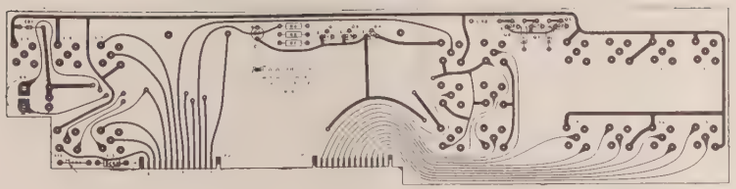
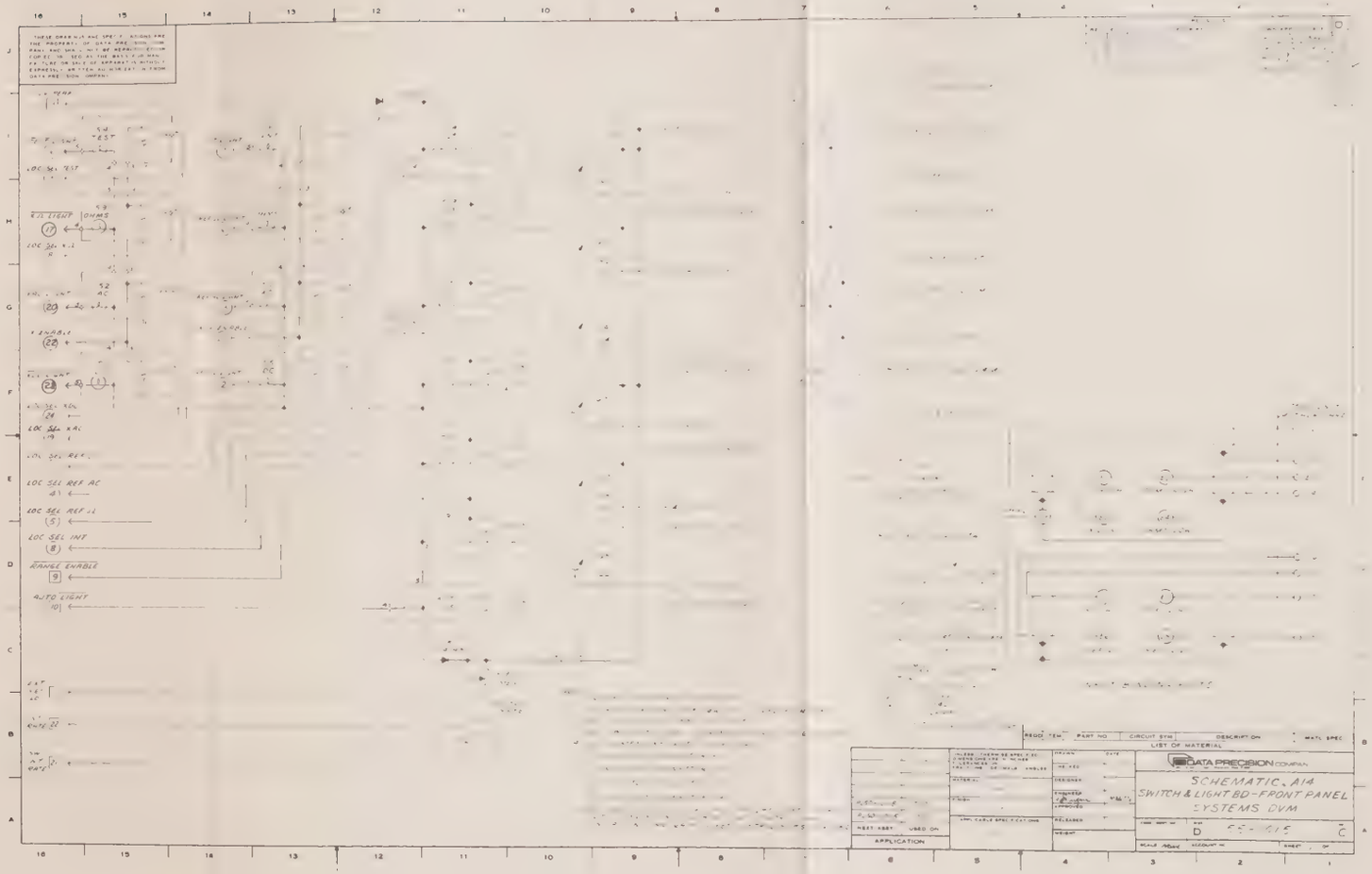


SWITCH & LIGHT BD - FRONT PANEL P.C. ASSY
PL50-1015, REV. A

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 15μf, 10V	23-441003
CR1	DIODE 1N4148	24-110001
CR2	DIODE 1N4004	24-104004
Q1,3,4,5,7,8	TRANSISTOR MPS-A13	24-240A13
R1,2,4,5,7,8	RESISTOR, 100K, ¼W, 5%, C.C.	22-021049
R9	POTENTIOMETER, 1 MEG	22-58-1031



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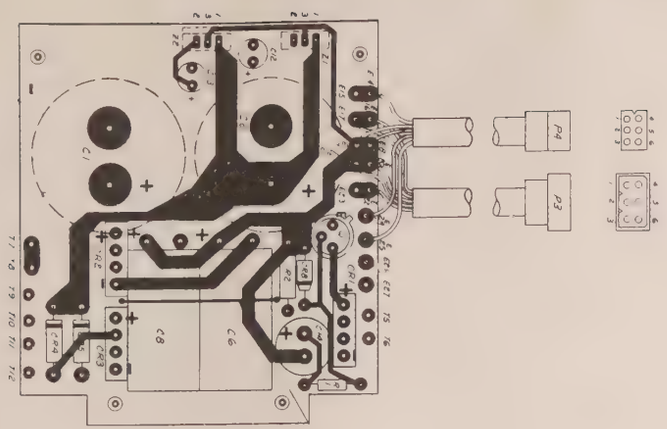
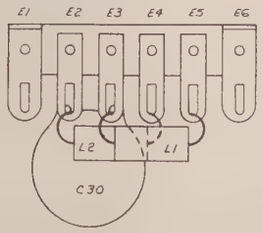


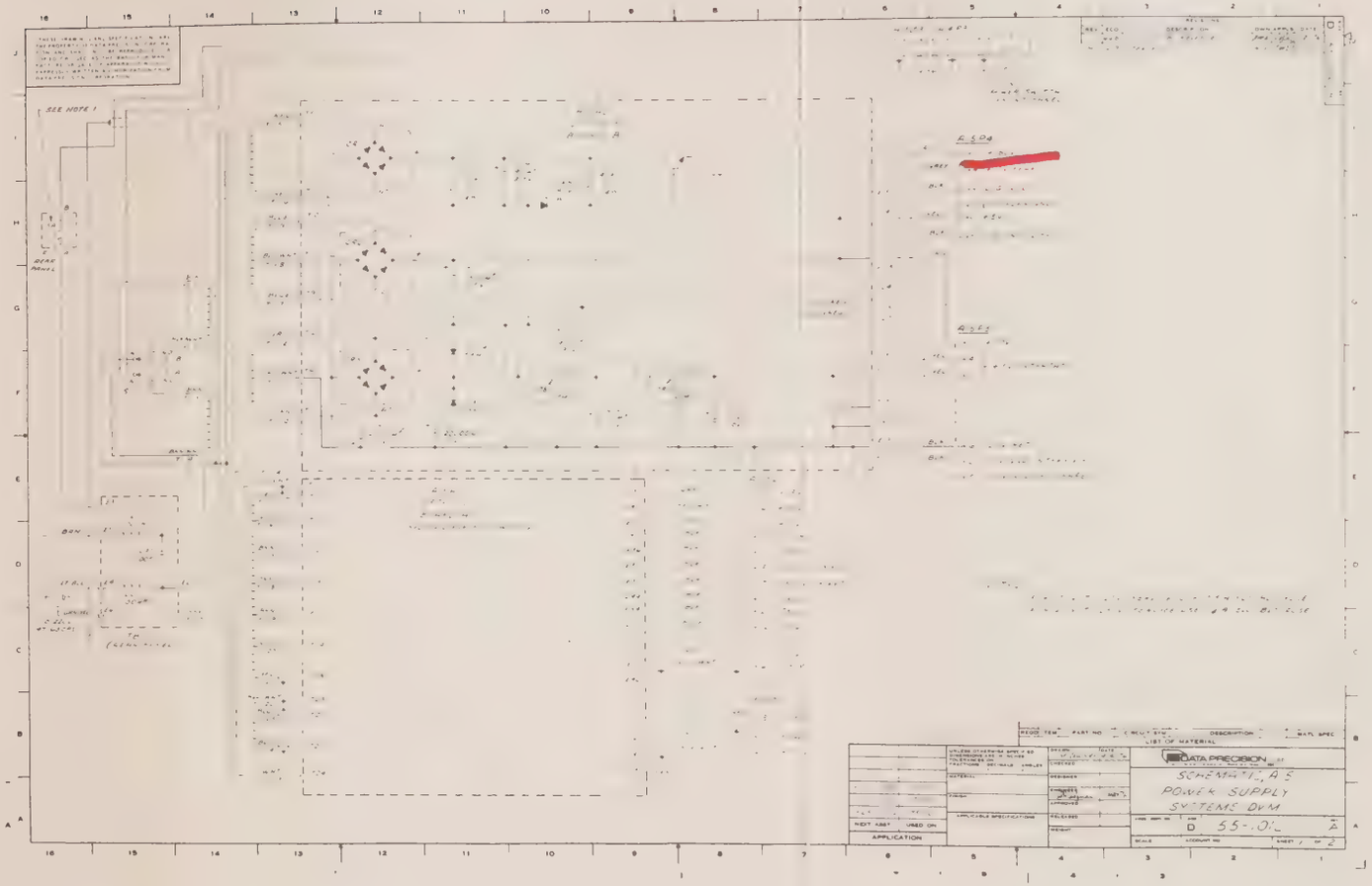
POWER SUPPLY BOARD B P.C. ASSY
PL50-1013 REV. D

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A15P4	CABLE ASSY	C58-1045
A15P3	CABLE ASSY	C58-1044
C1	CAPACITOR, 2300 µf, 35V	23-58-1035-1
C2	2200 µf, 10V	23-58-1035-2
C6	470 µf, 35V	23-620013
C8	2200 µf, 10V	23-620014
C12,13	15 µT, 10V	23-441003
C14	4.7 µf, 315V, ALUM.	23-620004
CR1,2,3	DIODE BRIDGE, 400V	24-100021
CR4,5	DIODE S3A05	24-10225-030
CR8	DIODE 180V, 5%, 1W	24-121008
Q1	TRANSISTOR 2N3440	24-203440
R1	RESISTOR, 47K, ¼W, 10%, C.C.	22-024739
R2	RESISTOR, 510K, ¼W, 5%, C.C.	22-025149
Z1,2	VOLTAGE REGULATOR	24-307805

POWER SUPPLY TERMINAL STRIP
PL50-1062, REV. A

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C30	CAPACITOR, 0.005 µf, 1.4KV	23-118010
L1,2	INDUCTOR, 100mH	25-100101
TB1	TERMINAL STRIP	25-762001





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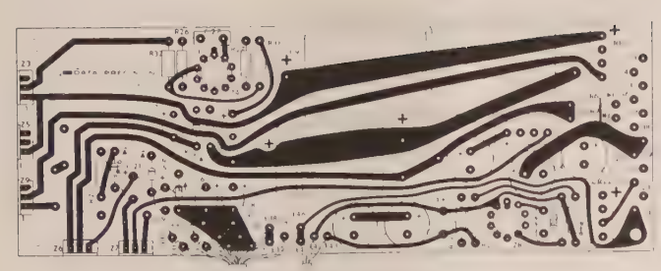
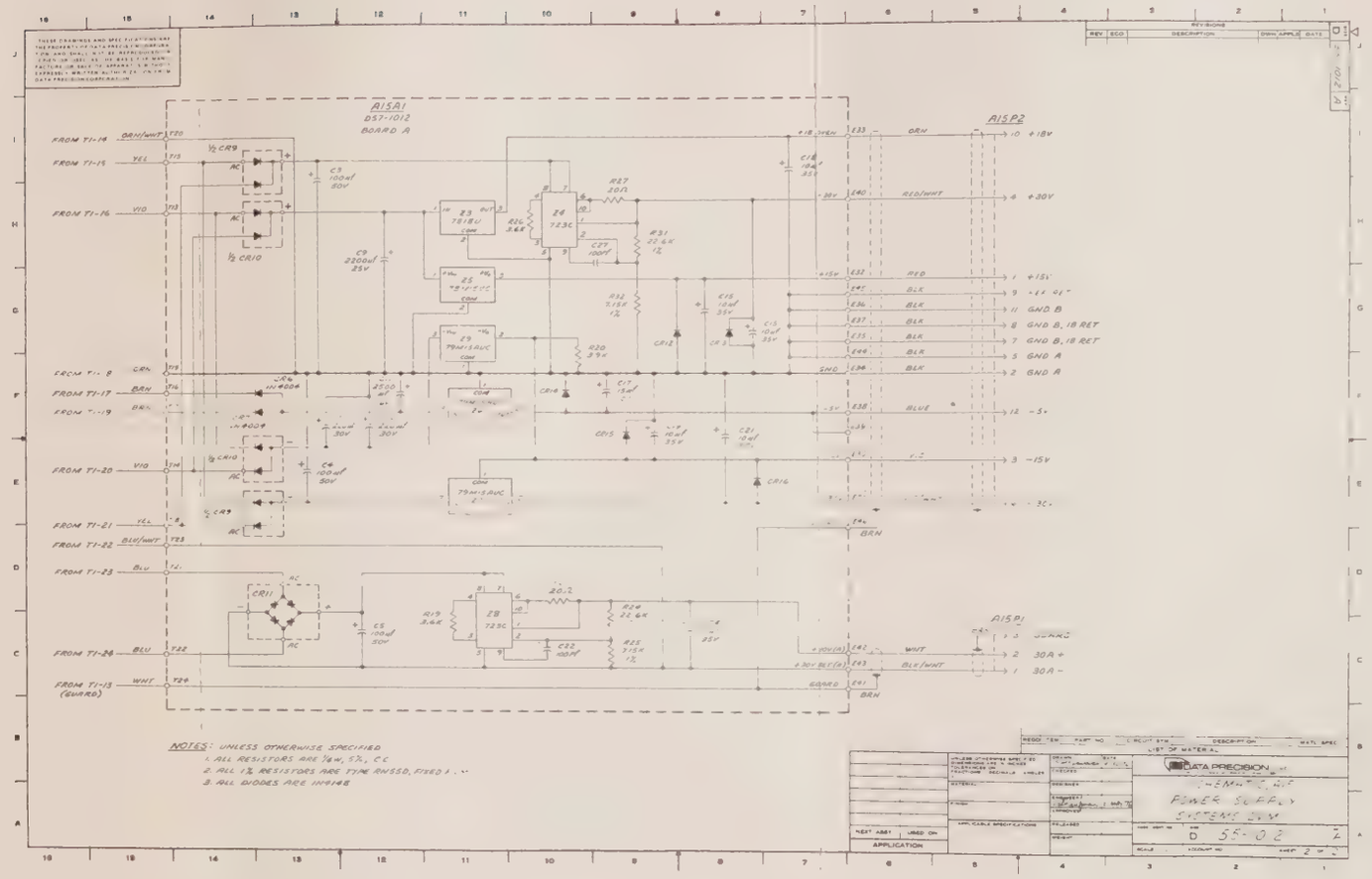


POWER SUPPLY BOARD A P.C. ASSY
PL50-1012 REV. C

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A15P1	CABLE ASSY	C58-1046
A15P2	CABLE ASSY	C58-1047
C3,4,5	CAPACITOR, 100 µf, 50V	23-620012
C7,10	220 µf, 35V	23-620006
C15,16,18,19,21	10 µf, 35V	23-441002
C17	15 µf, 10V	23-441003
C9	2200 µf, 25V	23-610017
C11	2500 µf, 16V, 10%	23-620005
C22,27	100pf, DM15	23-311011
C24	CAPACITOR, 1 µf, 35V	23-441001
CR6,7	DIODE 1N4004	24-104004
CR9,10,11	DIODE BRIDGE	24-100021
CR12 thru CR16	DIODE 1N4148	24-110001
R19,26	RESISTOR, 3.6K, ¼W, 5%, C.C.	22-023629
R21,27	20Ω, ¼W, 5%, C.C.	22-022009
R20	3.9K, ¼W, 5%, C.C.	22-023929
R24,31	22.6K, 1%, RN55D	22-332262
R25,32	RESISTOR, 7.15K, 1%, RN55D	22-337151
Z3	VOLTAGE REGULATOR	24-307818
Z6	VOLTAGE REGULATOR	24-379M05
Z7,Z9	VOLTAGE REGULATOR	24-379M15
Z5	VOLTAGE REGULATOR	24-378M15
Z4,8	I.C. 723C	24-300723



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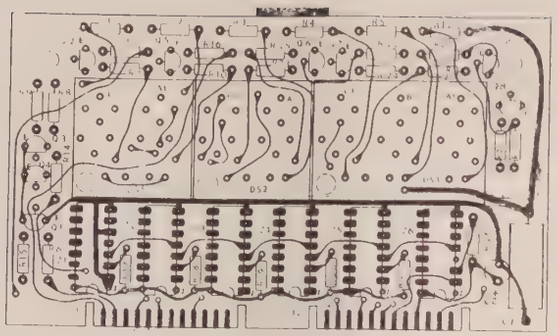
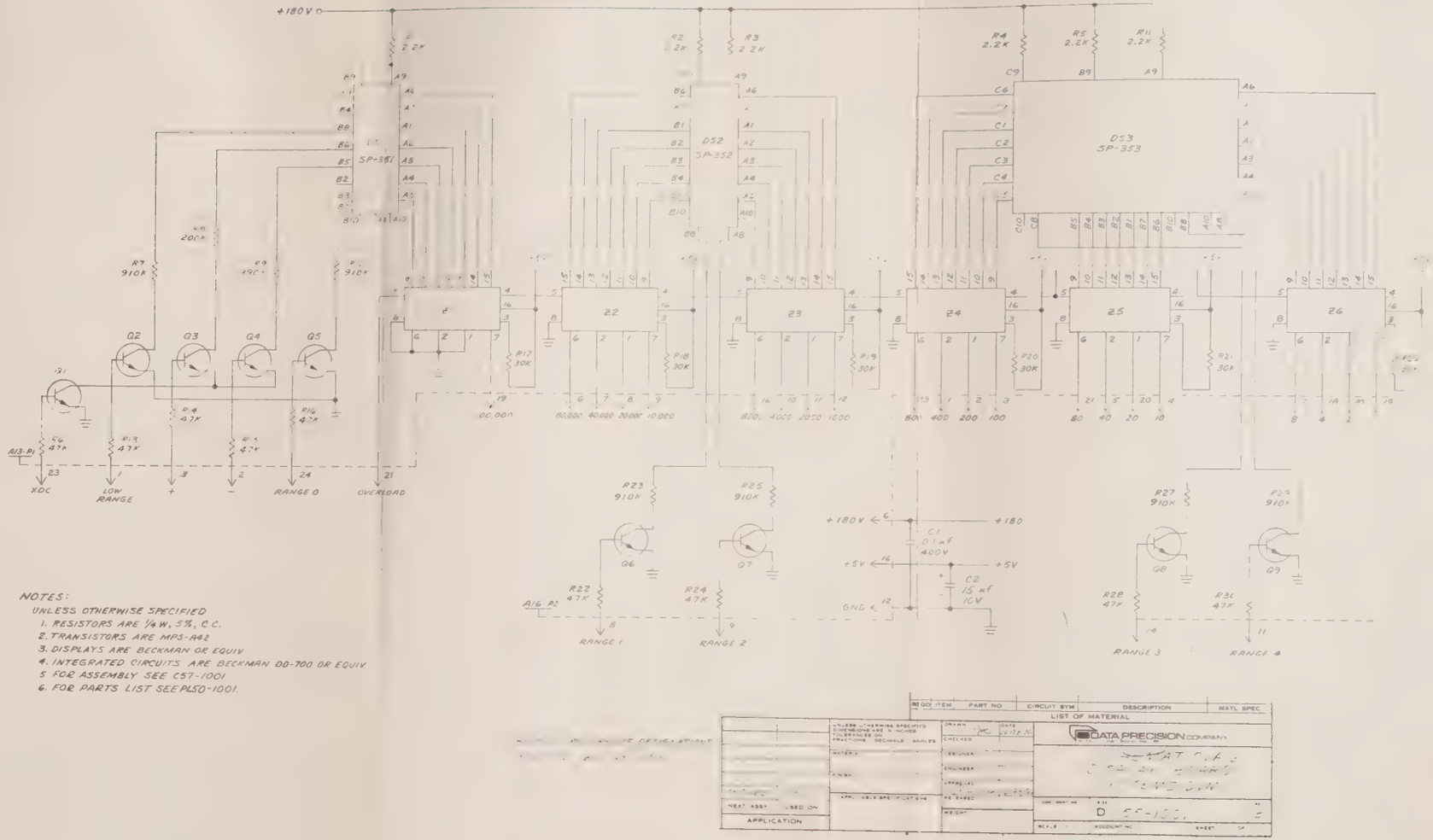


DIGITAL DISPLAY P.C. ASSY
PL50-1001, REV. A

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 0.1 µf, 400V, MYLAR	23-240001
C2	CAPACITOR, 15 µf, 10V, TANT	23-441003
DS1	DISPLAY SP-351	25-210351
DS2	DISPLAY SP-352	25-210352
DS3	DISPLAY SP-353	25-210353
Q1,2,3,4,5,6,7,8,9	TRANSISTOR, MPS-A42	24-230A42
R1,2,3,4,5,11	RESISTOR, 2.2K, ¼W, 5%, C.C.	22-022229
R6,13,14,15,16,22 R24,28,30	47K	22-024739
R7,10,23,25,27,29	910K	22-029149
R8	RESISTOR, 200K, ¼W, 5%, C.C.	22-022049
R9	390K, ¼W, 5%, C.C.	22-023949
R17,18,19,20,21,26	30K, ¼W, 5%, C.C.	22-023039
Z1,2,3,4,5,6	I.C. DD700, DM8880N, OR N5880B	24-A08880



NOTES:
UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE ¼W, 5%, C.C.
2. TRANSISTORS ARE MPS-A42
3. DISPLAYS ARE BECKMAN OR EQUIV
4. INTEGRATED CIRCUITS ARE BECKMAN DD-700 OR EQUIV
5. FOR ASSEMBLY SEE C57-1001
6. FOR PARTS LIST SEE PL50-1001.

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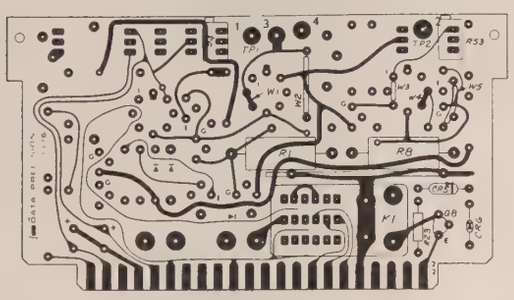
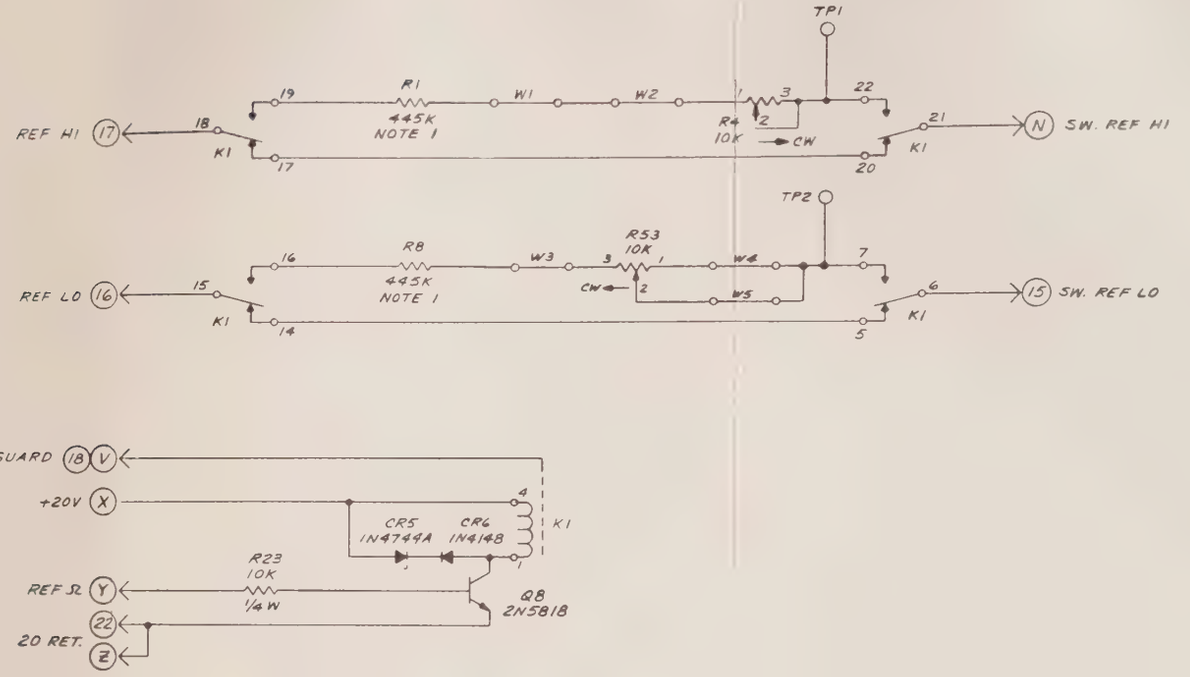


100V.F.S. REF. DC CONDITIONING
REF DC 05 OPTION P.C. ASSY
PL50-1079, REV. B

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
R1,8	RESISTOR,PRECISION, 445K	22-58-1012G21
R4,53	RESISTOR, TRIM, 10K	22-681007
R23	RESISTOR, 10K, ¼W, 5%	22-021039
CR5	DIODE,ZENER, 1N4744A	24-121103
CR6	DIODE,SWITCH, 1N4148	24-110001
K1	RELAY, 6 FORM C	25-171005
Q8	TRANSISTOR, 2N5818	24-235818



NOTES:
UNLESS OTHERWISE SPECIFIED –
1. RESISTORS INDICATED ARE A MATCHED SET PER S.C.D. B58-1012G21.

DATA PRECISION CORP

SCHEMATIC, 100V F.S.
REF DC CONDITIONING
(REF DC05) OPTION A1

	SIZE C	55-1036	REV A
SCALE ~	ACCOUNT NO	SHEET 1 OF 1	

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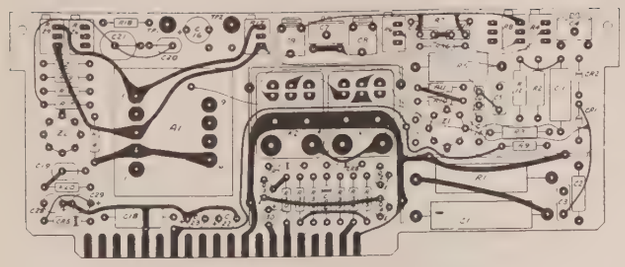
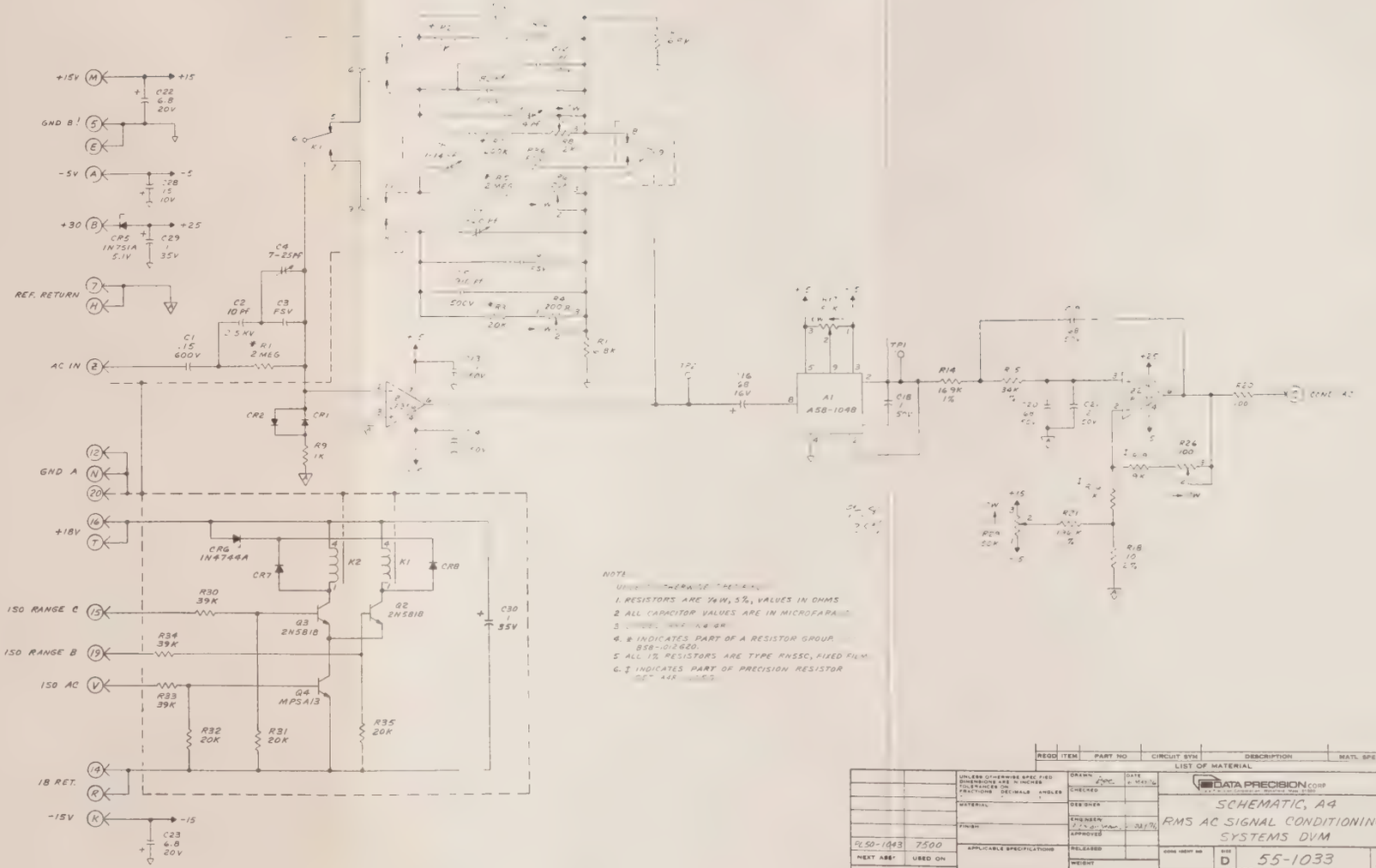


RMS AC SIGNAL CONDITIONING P.C. ASSEMBLY
PL50-1043, REV. C

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A1	RMS TO DC CONVERTER	A58-1048
C1	CAPACITOR,POLYCARB,0.15 µf,600V	23-510021
C2	CAPACITOR, 10pf, 2.5KV	23-711002
C4	CAPACITOR,VARIABLE,7-25pf,CERM	23-810000
C5	CAPACITOR, 910pf, 500V	23-311027
C7	CAPACITOR,VARIABLE,10-60pf,CERM	23-810003
C8,9	CAPACITOR,VARIABLE,1-14pf,GLASS	23-820000
C10	CAPACITOR, 82pf, 500V	23-310021
C11	CAPACITOR, 0.01 µf, 50V	23-510024
C12	CAPACITOR, 5pf, 500V	23-310004
C13,14	CAPACITOR, 0.01 µf, 150V	23-111006
C16	CAPACITOR, 68 µf, 15V MIN.	23-442004
C18	CAPACITOR, 1.5 µf, 50V	23-510003
C19,20	CAPACITOR, 0.68 µf, 50V	23-510019
C21	CAPACITOR, 2 µf, 50V	23-510002
C22,23	CAPACITOR, 6.8 µf, 20V	23-441005
C28	CAPACITOR, 15 µf, 10V	23-441003
C29,30	CAPACITOR, 1 µf, 35V	23-441001
CR1,2,7,8	DIODE, 1N4148	24-110001
CR5	DIODE,ZENER,1N751A,5.1V	24-120073
CR6	DIODE,ZENER,1N4744A	24-121103
K1,2	RELAY, 2 FORM C	25-171002
Q2,3	TRANSISTOR, 2N5818	24-235818
Q4	TRANSISTOR, MPS-A13	24-230A13
R1,2,3,5,7	RESISTOR SET, GROUP 20 2 MEG (R1) 2K (R2) 20K (R3) 200K (R7) 2 MEG (R5)	22-58-1012G20
R4	RESISTOR, TRIM, 200 Ω	22-681011
R6	RESISTOR, TRIM, 20K	22-681008
R8	RESISTOR, TRIM, 2K	22-681005
R9	RESISTOR, 1K, ¼W, 5%	22-021029
R10,11	RESISTOR, 6.8K, ¼W, 5%	22-026829
R12,18	RESISTOR,10Ω,2%,SEMI-PRECISION	22-121000
R14	RESISTOR, 16.9K, 1%, RN55C	22-341692
R15	RESISTOR, 34K, 1%, RN55C	22-343402
R16,R19	RESISTOR SET, PRECISION 1K (R16) 9K (R19)	22-48-1005G1
R17,29	RESISTOR,TRIMMER, 50K	22-681009
R20	RESISTOR, 100 Ω, ¼W, 5%	22-021019
R21	RESISTOR, 196K, 1%, RN55C	22-341963
R26	RESISTOR,TRIMMER,100 Ω	22-681002
R30,33,34	RESISTOR, 39K, ¼W, 5%	22-023939
R31,32,35	RESISTOR, 20K, ¼W, 5%	22-022039
Z1	I.C., OP. AMP, LF356	24-420356
Z2	I.C., OP. AMP, OP-07C	24-420007



REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC
LIST OF MATERIAL					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS DECIMALS ANGLES	DRAWN	DATE	DATA PRECISION CORP.
	CHECKED		SCHEMATIC, A4
MATERIAL	DESIGNED		RMS AC SIGNAL CONDITIONING
FINISH	ENGINEER		SYSTEMS DVM
PL50-1043 7500	APPROVED		
NEXT ASS'Y USED ON	RELEASED		SIZE D 55-1033 REV B
APPLICATION	WEIGHT		SCALE ~ ACCOUNT NO SHEET 1 OF 1

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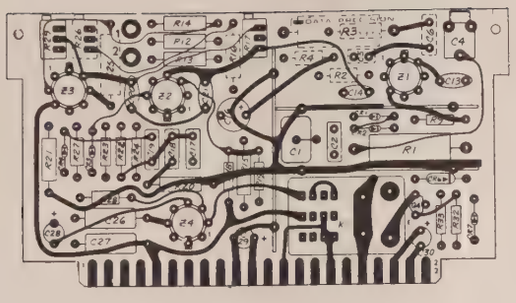

REF. AC SIGNAL CONDITIONING P.C. ASSY (BASIC)
PL50-1028, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 0.15 µf, 400V	23-510025
C2	10pf, 500V, DM15	23-311001
C4	VAR, 1-14pf, f67	23-820000
C17	150pf, 5%, DM15	23-311015
C13,14,20,21	.01 µf, CERM	23-111006
C18,19	5pf, 10%, DM10	23-310004
C16	68 µf, 20%, 15V, TANT	23-442004
C26	1 µf, 10%, 50V	23-510001
C27	0.68 µf, 10%, 50V	23-510019
C28,29	6.8 µf, 20V, TANT	23-441005
C30	CAPACITOR, 1 µf, 35V, TANT	23-441001
CR1,2,3,4,7	DIODE, 1N4148	24-110001
CR6	DIODE, 1N4744A	24-121103
K1	RELAY, 4 FORM C	25-171004
Q4	TRANSISTOR, MPSA13	24-230A13
R1	RESISTOR, 1M	22-58-1012G8
R9	RESISTOR, 1K, ¼W, C.C.	22-021029
R12	RESISTOR, 5K	22-58-1012G9
R13	RESISTOR, 10K	22-58-1012G9
R14,R15	RESISTOR, 25K	22-58-1012G (*)
R18	RESISTOR, 49.9Ω, 1%, RN55C	22-3449R9
R19	150K, 1%, RN55D	22-331503
R22	10K, 1%, RN55C	22-341002
R23,24	100K, ¼W, 5%	22-021049
R27,28	26.7K, 1%, RN55C	22-341002
R32	20K, ¼W, 5%	22-022039
R33	39K, ¼W, 5%	22-023939
R17	RESISTOR,TRIMMER, 50K	22-681009
R29	RESISTOR,TRIMMER, 20K	22-68-1008
R20	RESISTOR, 2740Ω	22-58-1012G18
R21	RESISTOR, 2470Ω	22-58-1012G18
Z1	I.C., OP. AMP., LM356H	24-420356
Z2	I.C., OP. AMP., CM301AH	24-420301
Z3,4	I.C., OP. AMP., OP-07C	24-420007

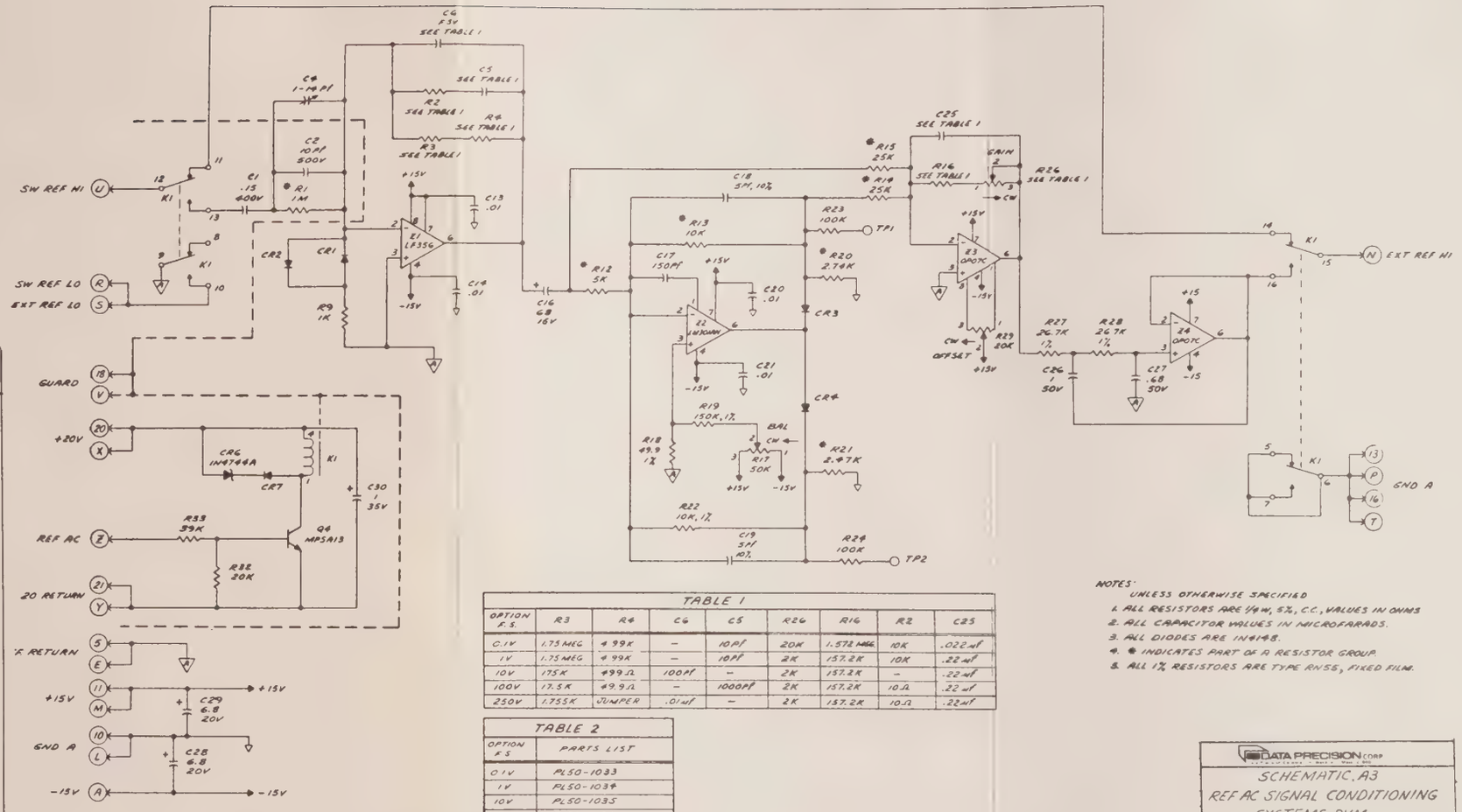

TABLE 1

OPTION F.S.	R3	R4	C6	C5	R26	R16	R2	C25
0.1V	1.75 MEG	4.99K	–	10pf	20K	1.572 MEG	10K	.022 uf
1V	1.75 MEG	4.99K	–	10pf	2K	157.2K	10K	.22 uf
10V	175K	499Ω	100pf	–	2K	157.2K	–	.22 uf
100V	17.5K	49.9Ω	–	1000pf	2K	157.2K	10Ω	.22 uf
250V	1.755K	JUMPER	.01 uf	–	2K	157.2K	10Ω	.22 uf

TABLE 2

OPTION F.S.	PARTS LIST
0.1V	PL50-1033
1V	PL50-1034
10V	PL50-1035
100V	PL50-1036
250V	PL50-1061

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5%, C.C., VALUES IN OHMS
2. ALL CAPACITOR VALUES IN MICROFARADS.
3. ALL DIODES ARE IN4148.
4. * INDICATES PART OF A RESISTOR GROUP.
5. ALL 1% RESISTORS ARE TYPE RN55, FIXED FILM.

DATA PRECISION CORP
SCHEMATIC, A3
REF AC SIGNAL CONDITIONING
SYSTEMS DVM
SIZE D | 55-1028 | REV —
SCALE — | ACCOUNT NO | SHEET 1 OF 1

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THE FOLLOWING OPTIONS USE THE BASIC P/L (PL50-1028)
IN ADDITION TO THE FOLLOWING PARTS FOR EACH OPTION

REF. AL SIGNAL CONDITIONING
0.1V OPT. (01)
PL50-1033 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C5	CAPACITOR, 10pf, 10%, DM10	23-311001
C25	CAPACITOR, .022 μf, 5%, 50V	23-510016
R1	RESISTOR, 1 MEG	22-58-1012G8
R3	RESISTOR, 1.75 MEG	22-58-1012G8
R4	RESISTOR, 4.99K, 1%, RN55C	22-344991
R14,15	RESISTOR, 25K	22-58-1012G11
R16	RESISTOR, 1.572 MEG	22-58-1012G11
R26	RESISTOR,TRIMMER, 20K	22-681008
R2	RESISTOR, 10K, ¼W. 5%	22-021039

REF. AC SIGNAL CONDITIONING
1V OPT. (02)
PL50-1034 REV.-

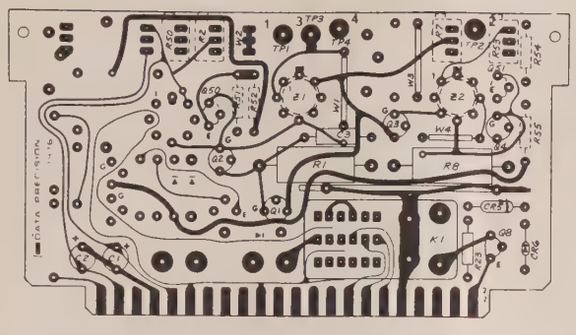
REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C5	CAPACITOR, 10pf, 10%, DM10	23-311001
C25	CAPACITOR, .22 μf, 50V	23-510017
R1	RESISTOR, 1 MEG	22-58-1012G8
R3	RESISTOR, 1.75 MEG	22-58-1012G8
R4	RESISTOR, 4.99K, 10%, RN55C	22-344991
R14,15	RESISTOR 25K	22-58-1012G10
R16	RESISTOR, 157.2K	22-58-1012G10
R26	RESISTOR,TRIMMER, 2K	22-681005
R2	RESISTOR, 10K, ¼W, 5%	22-021039

REF. AC SIGNAL CONDITIONING
10V OPT. (03)
PL50-1035 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C6	CAPACITOR, 100pf, 5%, DM15	23-311011
C25	CAPACITOR, .22 μf, 50V	23-510017
R1	RESISTOR, 1 MEG	22-58-1012G8
R3	RESISTOR, 175 MEG	22-58-1012G8
R4	RESISTOR, 499Ω, 1%, RN55C	22-344990
R14,15	RESISTOR, 25K	22-58-1012G10
R16	RESISTOR 157.2	22-58-1012G10
R26	RESISTOR,TRIMMER 2K	22-681005

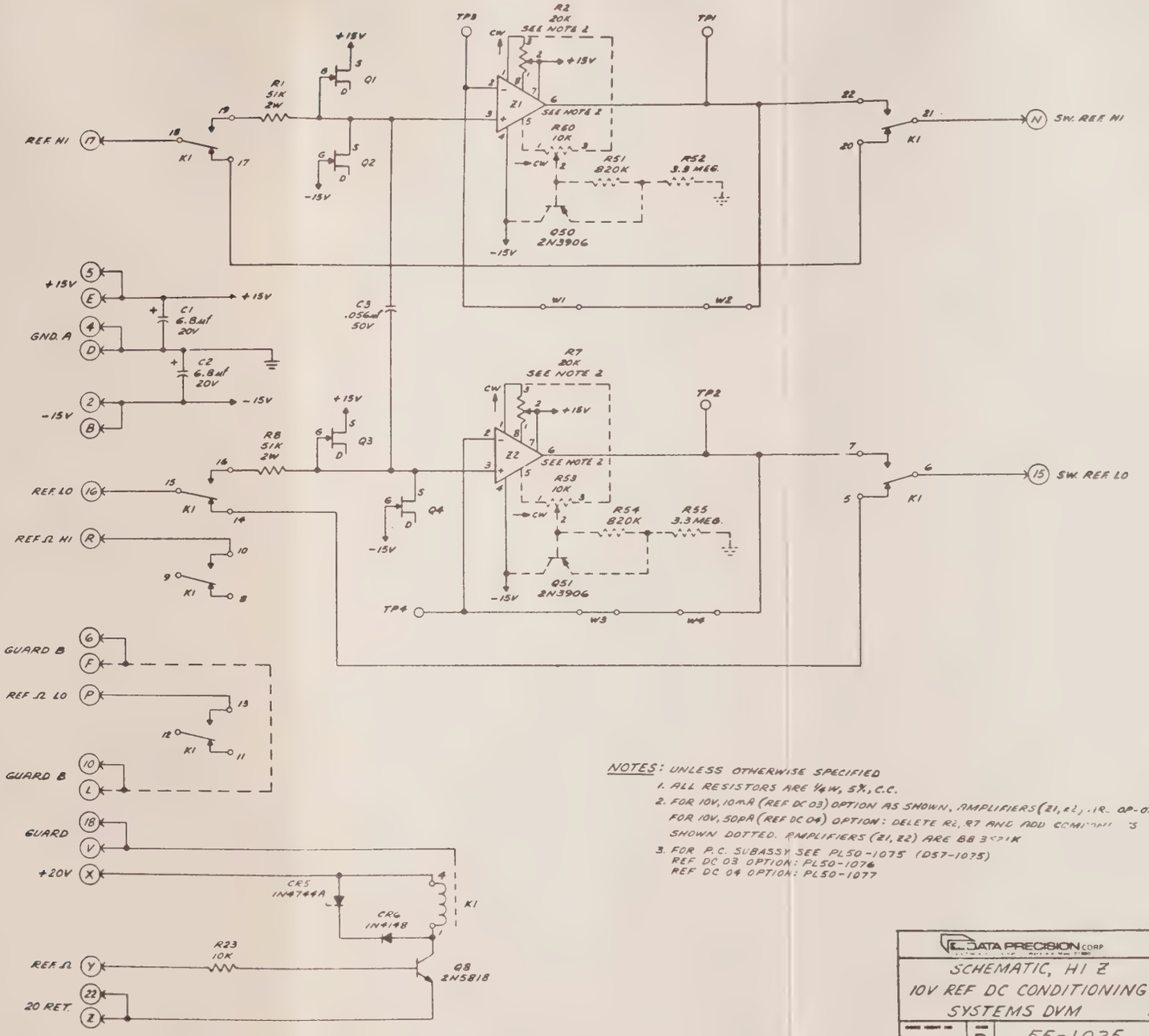
REF. AC SIGNAL CONDITIONING
100V OPT (04)
PL50-1036 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C5	CAPACITOR, 1000pf, 5%, DM10	23-311002
C25	CAPACITOR, .22 μf, 50V	23-510017
R1	RESISTOR, 1 MEG	22-58-1012G8
R3	RESISTOR, 17.5K	22-58-1012G8
R4	RESISTOR, 49.9Ω, 1%, RN55C	22-3449R9
R14,15	RESISTOR 25K	22-58-1012G10
R16	RESISTOR 157.2	22-58-1012G10
R26	RESISTOR,TRIMMER 2K	22-681005
R2	RESISTOR 10Ω, ¼W	22-021009



H1 Z 10V REF. DC CONDITIONING P.C. ASSY (BASIC)
PL50-1075, REV. A

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1,2	CAPACITOR, 6.8 µf, 20V, TANT	23-441005
C3	CAPACITOR, 0.056 µf, 50V, POLYCARB	23-510020
CR5	DIODE,ZENER, 1N4744A	24-121103
CR6	DIODE,SWITCH, 1N4148	24-110001
K1	RELAY, 6 FORM C	25-171005
Q1,2,3,4	TRANSISTOR,FET,ORN DOT	24-48-1014-10
Q8	TRANSISTOR,NPN, 2N5818	24-235818
R1,8	RESISTOR, 51K, 2W, 5%, C.C.	22-055139-C
R23	RESISTOR, 10K, ¼W, 5%	22-021039



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5%, C.C.
2. FOR 10V, 10mA (REF DC 03) OPTION AS SHOWN, AMPLIFIERS (Z1, Z2), IR. OP-07C.
   FOR 10V, 500µA (REF DC 04) OPTION: DELETE R2, R7 AND ADD COMPONENTS SHOWN DOTTED. AMPLIFIERS (Z1, Z2) ARE BB 3521K
3. FOR P.C. SUBASSY SEE PL50-1075 (DS7-1075)
   REF DC 03 OPTION: PL50-1076
   REF DC 04 OPTION: PL50-1077

DATA PRECISION CORP
SCHEMATIC, HI Z
10V REF DC CONDITIONING
SYSTEMS DVM A1
SIZE D 55-1035 REV -
SCALE ~ ASSEMBLY NO SHEET 1 OF 1

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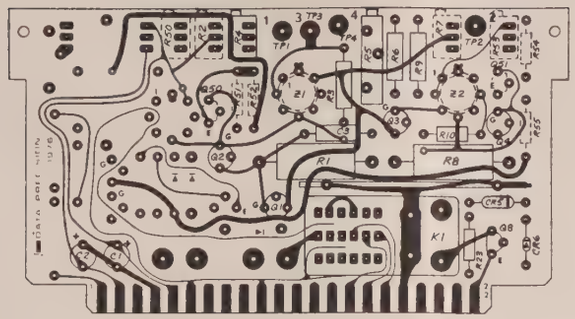
THE FOLLOWING OPTIONS USE THE BASIC P/L (PL50-1075)
IN ADDITION TO THE FOLLOWING PARTS FOR EACH OPTION.

H1 Z 10V REF. DC CONDITIONING
10V,10nA P.C. ASSY (REF. DC 03)
PL50-1076, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
R2,7	RESISTOR,TRIMMER, 20K	22-681008
Z1,2	I.C., OP. AMP, OP-07C	24-420007

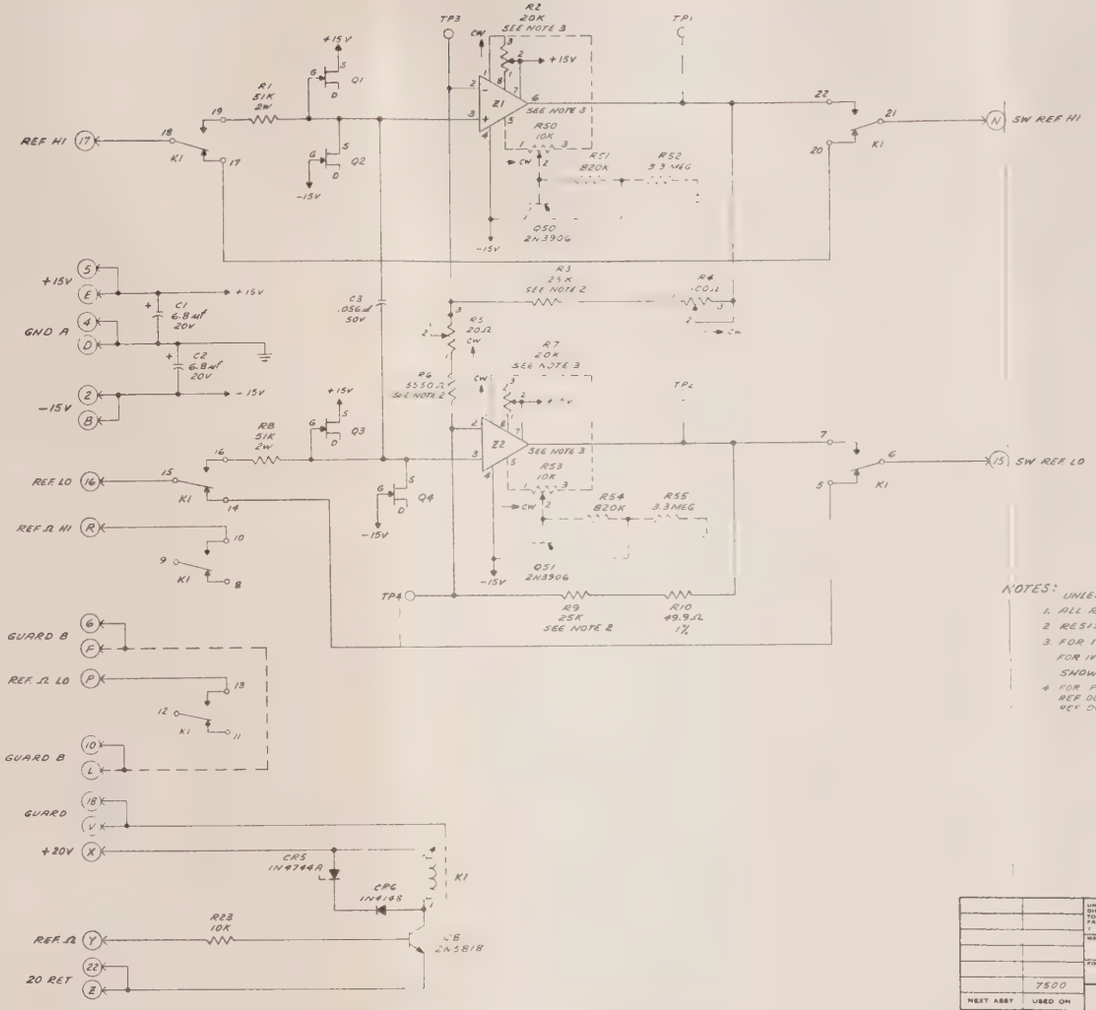
H1 Z 10V REF. DC CONDITIONING
10V,50pA P.C. ASSY (REF DC 04)
PL50-1077, REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
Q50,51	TRANSISTOR, PNP, 2N3906	24-243906
R50,53	RESISTOR,TRIMMER, 10K	22-681007
R51,54	RESISTOR, 820K, ¼W, 5%	22-028249
R52,55	RESISTOR, 3.3 MEG, ¼W, 5%	22-023359
Z1,2	I.C. OP AMP	24-423521



H1 Z 1V REF DC CONDITIONING P.C. SUB ASSY (BASIC)
PL50-1072, REV. A

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1,2	CAPACITOR, 6.8 µf, 20V, TANT	23-441005
C3	CAPACITOR, 0.056 µf, 50V, POLYCARB	23-510020
CR5	DIODE,ZENER, 1N4744A	24-121103
CR6	DIODE, SWITCH, 1N4148	24-110001
K1	RELAY, 6 FORM C	25-171005
Q1,2,3,4	TRANSISTOR,FET,ORN DOT	24-48-1014-10
Q8	TRANSISTOR,NPN, 2N5818	24-235818
R1,8	RESISTOR, 51K, 2W, 5%, C.C.	22-055139-C
R3,6,9	RESISTOR,SET,GROUP 17 25K (R3,R9) 5550 Ω(R6)	22-58-1012G17
R4	RESISTOR,TRIMMER,100 Ω	22-681002
R5	RESISTOR,TRIMMER, 20 Ω	22-681100
R10	RESISTOR, 49.9Ω, 1%, RN55C	22-3449R9
R23	RESISTOR, 10K, ¼W, 5%	22-021039



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5%, C.C
2. RESISTORS INDICATED ARE A MATCHED SET PER S.C.D. B58-1012 G17.
3. FOR 1VFS, 10mA OPTION (REF DC 01) AS SHOWN, AMPLIFIERS (Z1,Z2) ARE OP-07C
   FOR 1VFS, 50mA OPTION (REF DC 02) DELETE R2 & R7 AND ADD COMPONENTS
   SHOWN DOTTED. AMPLIFIERS (Z1, Z2) ARE BB-3521K
4. FOR P.C. SUBASSY SEE PL50-1072 (D57-1072)
   REF DC 01 OPTION: PL50-1073
   REF DC 02 OPTION: PL50-1074

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC
				LIST OF MATERIAL	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±. MATERIAL. FINISH. APPLICABLE SPECIFICATIONS.

DRAWN M. Schmidt 4-23-76. CHECKED. DESIGNER. ENGINEER W. Hamburger 4 AUG 76. APPROVED. RELEASED. WEIGHT.

DATA PRECISION

SCHEMATIC, HI Z
1V REF DC CONDITIONING
SYSTEMS DVM A1

NEXT ASSY	USED ON
	7500
APPLICATION	

SIZE D | DWG NO 55-1034 | REV —
SCALE — | ACCOUNT NO | SHEET 1 OF 1

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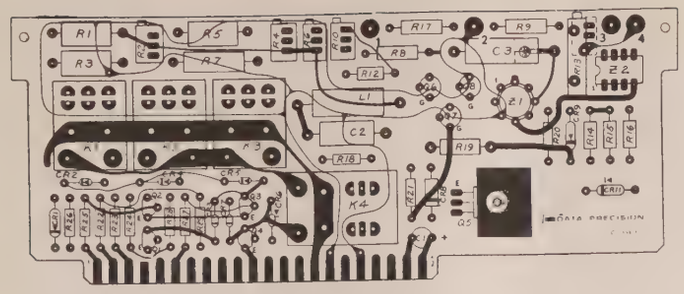
THE FOLLOWING OPTIONS USE THE BASIC P/L (PL50-1072)
IN ADDITION TO THE FOLLOWING PARTS FOR EACH OPTION

H1 Z REF. DC CONDITIONING
1VFS, 10mA P.C. ASSY (REF DC 01)
PL50-1073 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
R2,7	RESISTOR,TRIMMER, 20K	22-681008
Z1,2	I.C., OP. AMP, OP-07C	24-420007

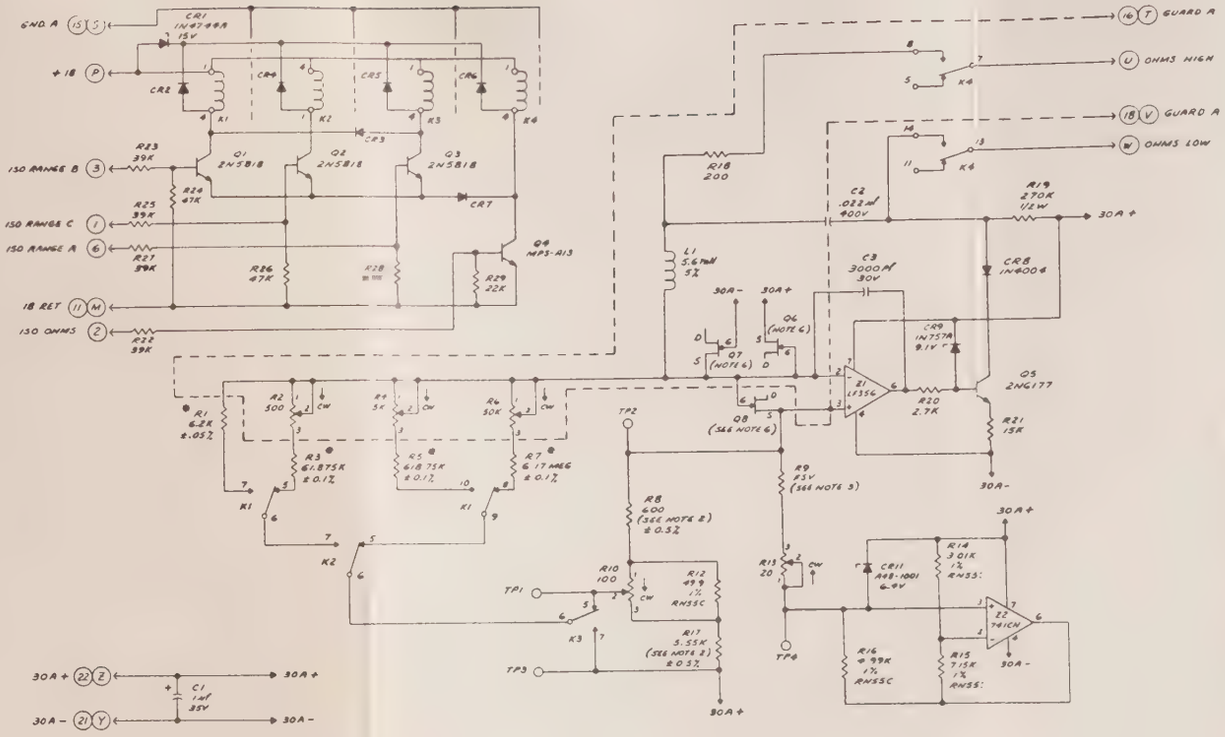
H1 Z REF DC CONDITIONING
1VFS, 50pA P.C. ASSY (REFDC02)
PL50-1074 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
Q50,51	TRANSISTOR, PNP, 2N3906	24-243906
R50,53	RESISTOR,TRIMMER,10K	22-681007
R51,54	RESISTOR, 820K, ¼W, 5%	22-028249
R52,55	RESISTOR, 3.3 MEG, ¼W, 5%	22-023359
Z1,2	I.C. OP. AMP	24-423521



OHMS CURRENT SOURCE P.C. ASSY
PL50-1010 REV. C

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 1 µf, 35V	23-441001
C2	CAPACITOR, .022 µf, 400V, POLYCARB	23-510015
C3	CAPACITOR, 3000pf, 30V, POLYSTY	23-550103
CR1	DIODE,ZENER, 1N4744A	24-121103
CR2,CR7	DIODE,SWITCHING, 1N4148	24-110001
CR8	DIODE,RECTIFIER, 1N4004	24-104004
CR9	DIODE,ZENER, 1N4739A	24-121102
CR11	DIODE, REF	24-48-1001
K1,2,3	RELAY, 2 FORM C	25-171002
K4	RELAY, 2 FORM C,HI VOLTAGE	25-58-1014
L1	INDUCTOR, 5.6 mH	25-100025
Q1,2,3	TRANSISTOR,NPN, 2N5818	24-235818
Q4	TRANSISTOR,MPS-A13,DARLINGTON	24-230A13
Q5	TRANSISTOR,POWER, 2N6177	24-226177
Q6,7,8	TRANSISTOR,FET,ORN DOT	24-48-1014-10
R1,3,5,7	RESISTOR SET, GROUP 6 6200Ω (R1) 61875Ω (R3) 618.75K (R5) 6.17 MEG (R7)	22-58-1012G6
R2	RESISTOR,TRIM, 500Ω	22-681003
R4	RESISTOR,TRIM, 5K	22-681006
R6	RESISTOR,TRIM, 50K	22-681009
R8,17	RESISTOR SET, GROUP 5 600Ω (R8) 5550Ω (R17)	22-58-1012G5
R10	RESISTOR,TRIM, 100Ω	22-681002
R12	RESISTOR, 49.9Ω, RN55C	22-3449R9
R13	RESISTOR,TRIM, 20Ω	22-681100
R14	RESISTOR, 3.01K, 1%, RN55C	22-343011
R15	RESISTOR, 7.15K, 1%, RN55C	22-347151
R16	RESISTOR, 4.99K, 1%, RN55C	22-344991
R18	RESISTOR, 200Ω, ¼W, 5%	22-022019
R19	RESISTOR, 270K, ½W, 5%	22-032749
R20	RESISTOR, 2.7K, ¼W, 5%	22-022729
R21	RESISTOR, 15K, ¼W, 5%	22-021539
R22,23,25,27	RESISTOR, 39K, ¼W, 5%	22-023939
R24,26,28	RESISTOR, 47K, ¼W, 5%	22-024739
R29	RESISTOR, 22K, ¼W, 5%	22-022239
Z1	I.C. LF356	24-420356
Z2	I.C. 741CN	24-400741



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5%, C.C., VALUES IN OHMS
2. R8 & R17 ARE A MATCHED SET, SEE SCD BSB-1012, GROUP 5.
3. SELECT FOR 6.20V, TP2 TO TP3 USING VALUES FROM TABLE 1.
4. ALL DIODES ARE IN9148
5. * INDICATES PART OF RESISTOR GROUP BSB-1012 G6
6. FETS Q6, Q7 & Q8 ARE A48-1014-10

TABLE 1
R9 SELECTION CHART

CR11 VOLTAGE TP3 - TP4	R9 VALUE OHMS ±1%
6.2006	0
6.2164	16.5
6.2321	32.4
6.2984	98.7
6.2643	64.9
6.2798	80.6
6.2998	95.3
6.3090	110
6.3228	124
6.3357	137
6.3486	150
6.3606	162
6.3723	174
6.3852	187
6.3981	200
6.4080	210
6.4188	221
6.4297	232
6.4404	243
6.4525	255
6.4644	267
6.4773	280
6.4911	294
6.4980	301
6.5059	

DATA PRECISION CORP.
SCHEMATIC, A2
OHMS CURRENT SOURCE
SYSTEMS DVM
D 55-1010 A

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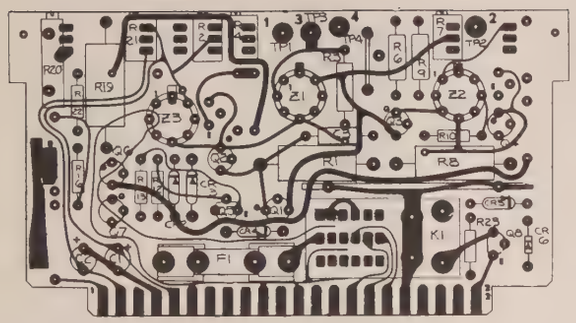
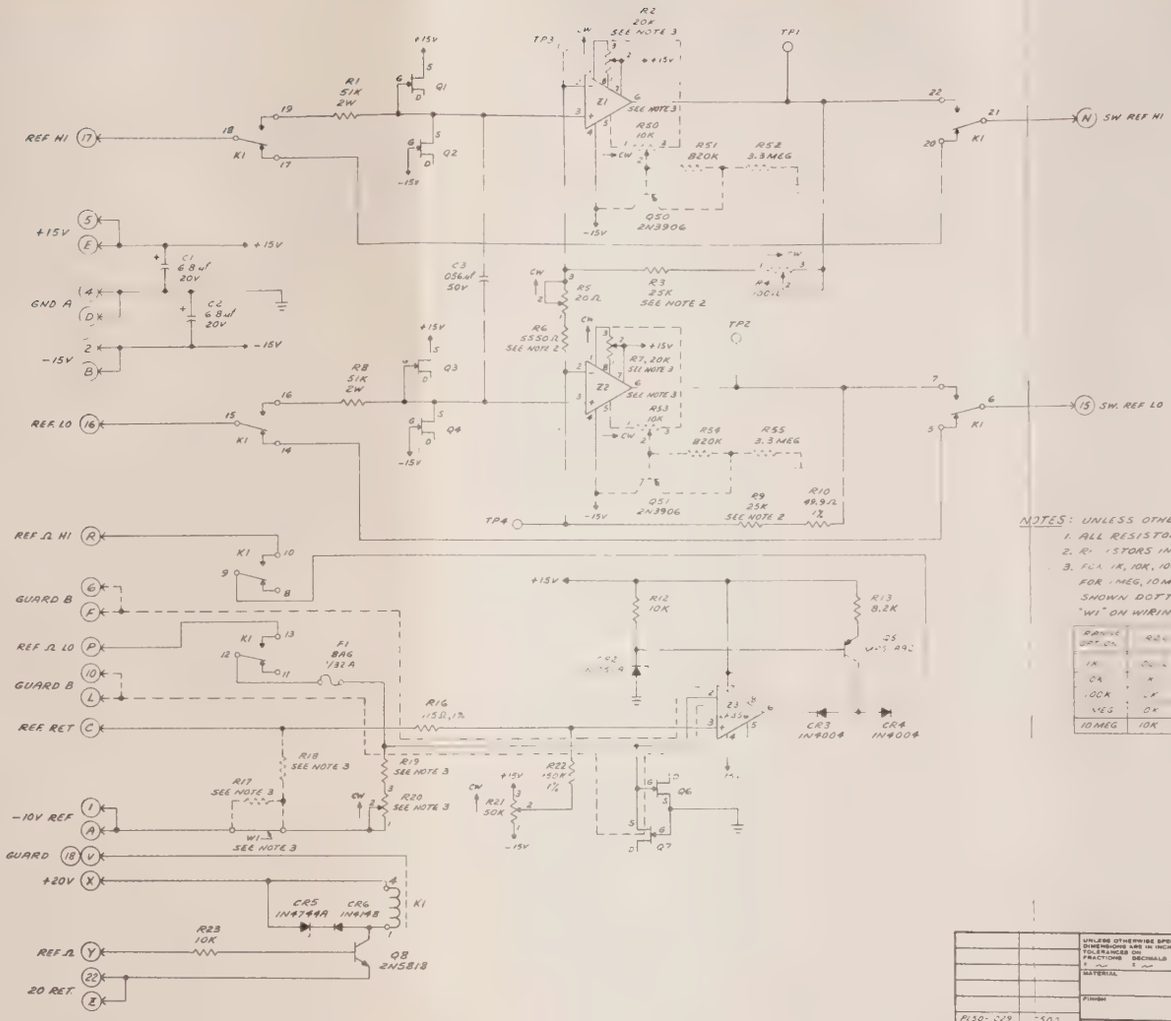


REF OHMS CONDITIONING P.C. ASSY (BASIC)
PL50-1029 REV. F

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1,2	CAPACITOR, 6.8µf, TANT	23-441005
C3	CAPACITOR, 0.056 µf, 50V, POLYCARB	23-510020
CR2	DIODE,ZENER, 1N751A	24-120073
CR3,4	DIODE,RECTIFIER, 1N4004	24-104004
CR5	DIODE,ZENER, 1N4744A	24-121103
CR6	DIODE,SWITCH, 1N4148	24-110001
F1	FUSE,1/32A,8AG or AGX	25-501010
K1	RELAY, 6 FORM C	25-171005
Q1,2,3,4,6,7	TRANSISTOR,FET,ORN DOT	24-48-1014-10
Q5	TRANSISTOR,PNP,MPS-A92	24-240A92
Q8	TRANSISTOR,NPN, 2N5818	24-235818
R1,8	RESISTOR, 51K, 2W, 5%, C.C.	22-055139
R3,6,9	RESISTOR SET,GROUP 17 25K (R3,R9) 5550Ω (R6)	22-58-1012G17
R4	RESISTOR,TRIM, 100Ω	22-681002
R5	RESISTOR,TRIM, 20Ω	22-681100
R10	RESISTOR, 49.9Ω, 1%, RN55C	22-3449R9
R12,23	RESISTOR, 10K, ¼W, 5%, C.C.	22-021039
R13	RESISTOR, 8.2K, ¼W, 10%, C.C.	22-028228
R16	RESISTOR, 115Ω, 1%, RN60C	22-371150
R21	RESISTOR,TRIM, 50K	22-681009
R22	RESISTOR, 150K, 1%, RN55D	22-331503
Z3	I.C. OP. AMP., LF356H	24-420356



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5%, CC
2. RESISTORS INDICATED ARE A MATCHED SET PER SCD B58-1012 G17
3. FOR 1K, 10K, 100K OPTIONS AS SHOWN, AMPLIFIERS (Z1, Z2) ARE OP-07C FOR 1MEG, 10MEG RANGE OPTIONS: DELETE R2, R7 & ADD COMPONENTS SHOWN DOTTED. AMPLIFIERS (Z1, Z2) ARE BB 3521K. CUT ETCH LINE "W1" ON WIRING SIDE OF BOARD WHEN INSTALLING R17.

RANGE OPTION	R2	R7	R8	R9	R10	CR5
					B58-1012	
1K	OMIT	996.0K		—	GROUP 2	OMIT
10K	1K	99.60K		—	GROUP 3	OMIT
100K	1K	996.0K	—	—	GROUP 14	OMIT
1MEG	10K	996.0K	89.1K	10.0K	GROUP 15	INSTALL
10MEG	10K	996.0K	99.0K	1.000K	GROUP 16	INSTALL

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN — DATE 4-26-76
CHECKED
DESIGNER
ENGINEER
APPROVED
RELEASED
WEIGHT

DATA PRECISION
SCHEMATIC, AI
REF. OHMS CONDITIONING
SYSTEMS DVM

PL50-029	-500
NEXT ASSY	USED ON
APPLICATION	

SIZE D | 55-1029 | REV A
SCALE ~ | ACCOUNT NO | SHEET 1 OF 1

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THE FOLLOWING OPTIONS USE THE BASIC P/L (PL50-1029)
IN ADDITION TO THE FOLLOWING PARTS FOR EACH OPTION

REF OHMS CONDITIONING
1K FS OPTION (02) P.C. ASSY
PL50-1037 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
R2,7	RESISTOR,TRIM 20K	22-681008
R19	RESISTOR, 9960Ω	22-58-1012G12
R20	RESISTOR,TRIM, 100Ω	22-681002
Z1,2	I.C., OP. AMP., OP-07C	24-420007

REF OHMS CONDITIONING
10K FS OPTION (03) P.C. ASSY
PL50-1038 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
R2,7	RESISTOR,TRIM, 20K	22-681008
R19	RESISTOR, 99.60K	22-58-1012G13
R20	RESISTOR,TRIM, 1K	22-681004
Z1,2	I.C., OP. AMP., OP-07C	24-420007

REF OHMS CONDITIONING
100K FS OPTION (04) P.C. ASSY
PL50-1039 REV.-

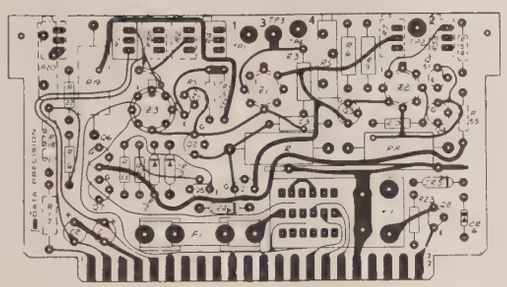
REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
R2,7	RESISTOR,TRIM, 20K	22-681008
R19	RESISTOR, 996.0K	22-58-1012G14
R20	RESISTOR,TRIM, 10K	22-681007
Z1,2	I.C. OP. AMP., OP-07C	24-420007

REF OHMS CONDITIONING
1 MEG FS OPTION (05) P.C. ASSY
PL50-1040 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
R17,18,19	RESISTOR SET, GROUP 15 89.1K (R17) 10.0K (R18) 996.0K (R19)	22-58-1012G15
R20,50,53	RESISTOR,TRIM, 10K	22-681007
R51,54	RESISTOR, 820K, ¼W, 5%	22-028249
R52,55	RESISTOR, 3.3MEG, ¼W, 5%	22-023359
Q50,51	TRANSISTOR,PNP, 2N3906	24-243906
Z1,2	I.C. OP. AMP.	24-423521

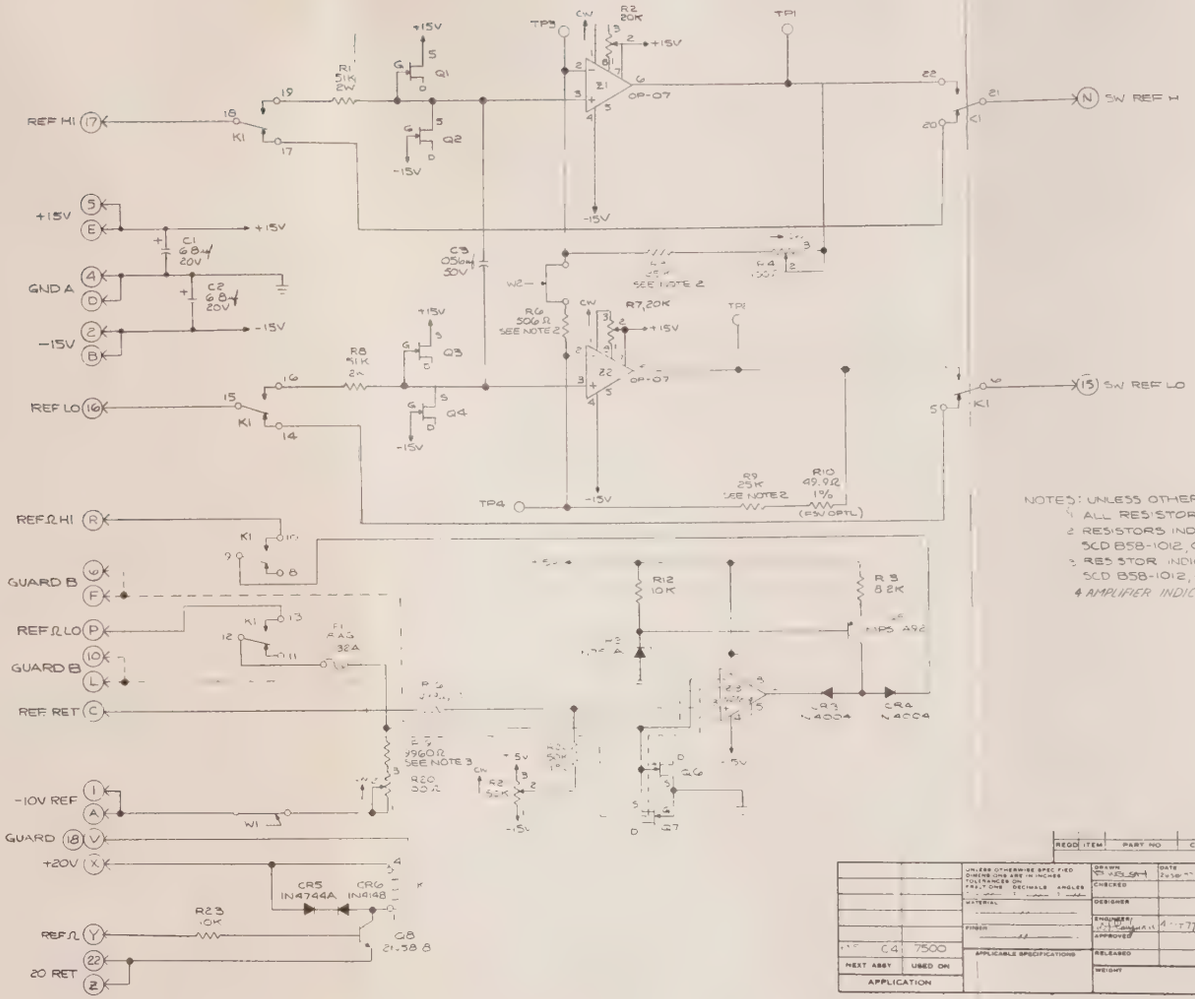
REF OHMS CONDITIONING
10 MEG FS OPTION (06) P.C. ASSY
PL50-1041 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
R17,18,19	RESISTOR SET,GROUP 16 99.0K (R17) 1.000K (R18) 996.0K (R19)	22-58-1012G16
R20,50,53	RESISTOR,TRIM, 10K	22-681007
R51,54	RESISTOR, 820K, ¼W, 5%	22-028249
R52,55	RESISTOR, 3.3MEG, ¼W, 5%	22-023359
Q50,51	TRANSISTOR,PNP, 2N3906	24-243906
Z1,2	I.C. OP. AMP.	24-423521



REF OHMS CONDITIONING 100
F.S. OPTION (RK01) P.C. ASSY
PL50-1104 REV. A.

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1,2	CAPACITOR, 6.8 µf, 20V, TANT	23-441005
C3	CAPACITOR, 0.056 µf, 50V, POLYCARB	23-510020
CR2	DIODE,ZENER, 1N751A	24-120073
CR3,4	DIODE,RECTIFIER, 1N4004	24-104004
CR5	DIODE,ZENER, 1N4744A	24-121103
CR6	DIODE,SWITCH, 1N4148	24-110001
F1	FUSE, 1/32A, 8AG or AGX	25-501010
K1	RELAY, 6 FORM C	25-171005
Q1,2,3,4,6,7	TRANSISTOR,FET,ORN DOT	24-48-1014-10
Q5	TRANSISTOR,PNP,H.V.,MPS-A92	24-240A92
Q8	TRANSISTOR,NPN, 2N5818	24-235818
R1,8	RESISTOR, 51K, 2W, 5%, C.C.	22-055139
R2,7	RESISTOR,TRIM, 20K	22-681008
R3,6,9	RESISTOR SET,GROUP 23 25K (R3,9) 506Ω (R6)	22-58-1012G23
R4,20	RESISTOR,TRIM, 100Ω	22-681002
R10,16	RESISTOR, 49.9Ω, 1%, RN55C	22-3449R9
R12,23	RESISTOR, 10K, ¼W, 5%	22-021039
R13	RESISTOR, 8.2K, ¼W, 10%	22-028228
R19	RESISTOR SET,GROUP 12 9960Ω (R19)	22-58-1012G12
R21	RESISTOR,TRIM, 50K	22-681009
R22	RESISTOR, 150K, 1%, RN55D	22-331503
Z1,2	I.C. OP. AMP., OP-07C	24-420007
Z3	I.C. OP. AMP.	24-58-1026



NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE 1/4W 5% C.C.
2 RESISTORS INDICATED ARE MATCHED SET PER SCD B58-1012, GROUP 23
3 RESISTOR INDICATED (R19) IS PER SCD B58-1012, GROUP 12
4 AMPLIFIER INDICATED (Z3) PER DSB-1026

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

DATA PRECISION

SCHEMATIC
REF. OHMS CONDITIONING
100Ω FS OPTION (RK01)

DRAWN	DATE	CODE IDENT NO	SIZE
CHECKED		81882	D
DESIGNER		DRAWING NO	REV
ENGINEER/ APPROVED		55-1043	A
RELEASED		SCALE	SHEET 1 OF 1
WEIGHT		ACCOUNT NO	

C4: 7500
NEXT ASSY | USED ON
APPLICATION

APPLICABLE SPECIFICATIONS

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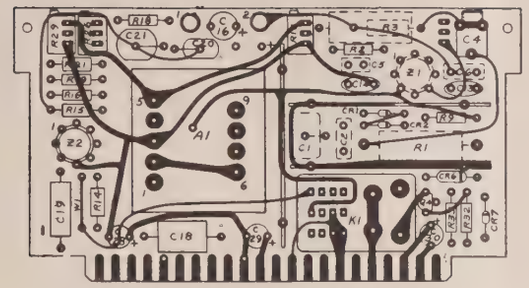

REF AC RMS SIGNAL CONDITIONING
P.C. ASSEMBLY (BASIC)
PL50-1089 REV. A

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A1	RMS TO DC CONVERTER	A58-1048
C4	CAPACITOR,VARIABLE, 1-14pf	23-820000
C13,14	CAPACITOR, .01 µf, CERAMIC	23-111006
C16	CAPACITOR, 68 µf, 15V MIN.	23-442004
C18	CAPACITOR, 1 µf, 50V	23-510001
C19,20	CAPACITOR, 0.68 µf, 50V	23-510019
C21	CAPACITOR, 2 µf, 50V	23-510002
C28,29	CAPACITOR, 6.8 µf, 25V, TANT	23-441005
C30	CAPACITOR, 1 µf, 35V, TANT	23-441001
CR1,2,7	DIODE,SWITCHING, 1N4148	24-110001
CR6	DIODE,ZENER, 1N4744A	24-121103
K1	RELAY, 4 FORM C	25-171004
Q4	TRANSISTOR,MPSA13	24-230A13
R9	RESISTOR, 1K, ¼W, 5%, C.C.	22-021029
R14	RESISTOR, 16.9K, 1%, RN55C	22-341692
R15	RESISTOR, 34K, 1%, RN55C	22-343402
R16,19	RESISTOR SET, GROUP 1 1K (R16) 9K (R19)	22-48-1005G1
R17,29	RESISTOR,TRIMMER, 50K	22-681009
R18	RESISTOR, 10Ω, 2%, SEMI-PREC.	22-121000
R21	RESISTOR, 196K, 1%, RN55C	22-341963
R26	RESISTOR,TRIMMER, 200Ω	22-681011
R32	RESISTOR, 20K, ¼W, 5%, C.C.	22-022039
R33	RESISTOR, 39K, ¼W, 5%, C.C.	22-023939
Z2	I.C. OP. AMP., OP-07C	24-420007

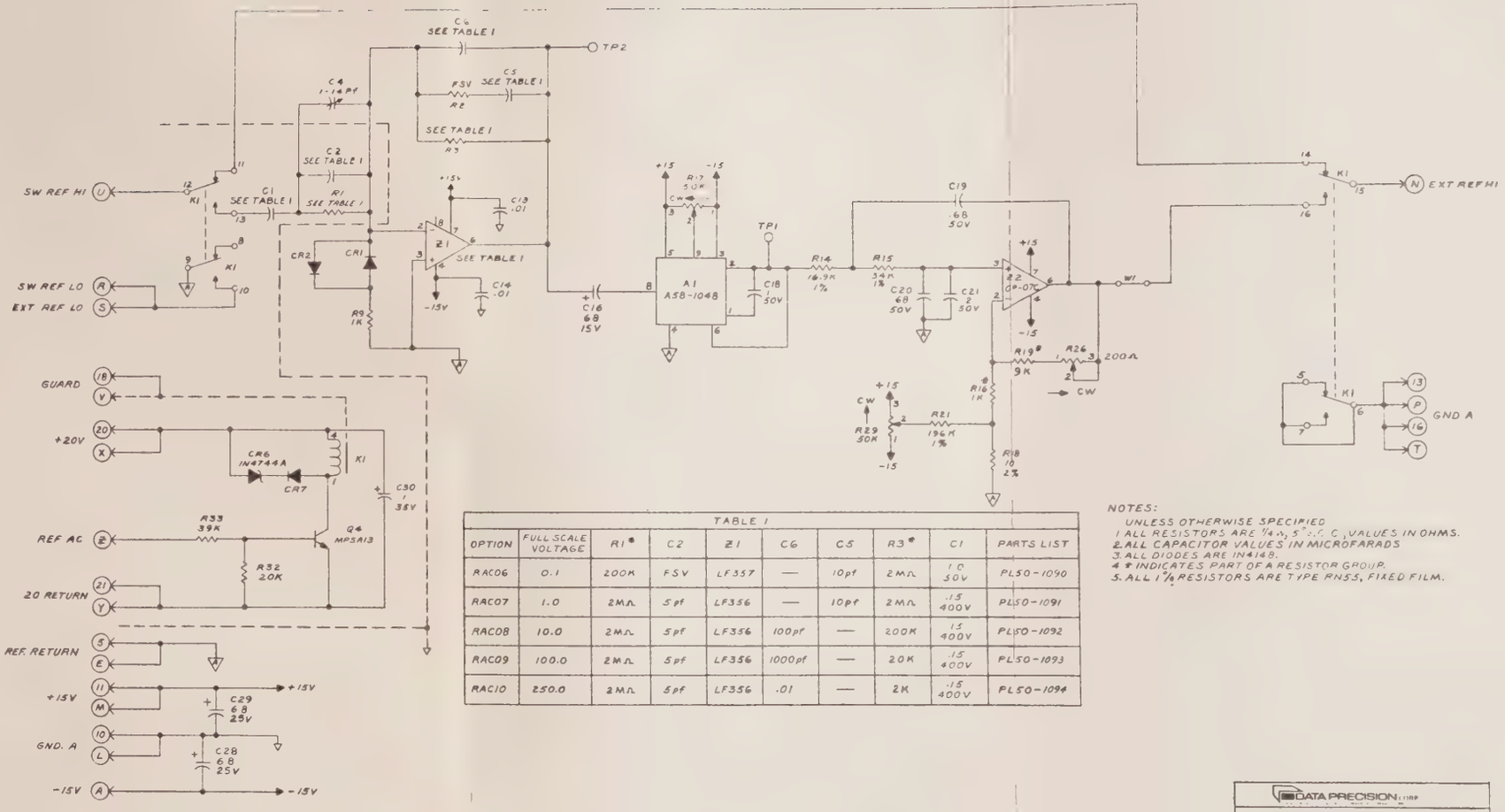

TABLE 1									
OPTION	FULL SCALE VOLTAGE	R1*	C2	Z1	C6	C5	R3*	C1	PARTS LIST
RAC06	0.1	200K	FSV	LF357	—	10pf	2MΩ	1.0 50V	PL50-1090
RAC07	1.0	2MΩ	5pf	LF356	—	10pf	2MΩ	.15 400V	PL50-1091
RAC08	10.0	2MΩ	5pf	LF356	100pf	—	200K	.15 400V	PL50-1092
RAC09	100.0	2MΩ	5pf	LF356	1000pf	—	20K	.15 400V	PL50-1093
RAC10	250.0	2MΩ	5pf	LF356	.01	—	2K	.15 400V	PL50-1094

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼ W, 5% C.C. VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS
3. ALL DIODES ARE IN4148.
4. * INDICATES PART OF A RESISTOR GROUP.
5. ALL 1% RESISTORS ARE TYPE RN55, FIXED FILM.

DATA PRECISION CORP.
SCHEMATIC, A3
REF. AC RMS SIGNAL CONDITIONING
SYSTEMS DVM
81692 | D | 55-1039

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THE FOLLOWING OPTIONS USE THE BASIC P/L (PL50-1089)
IN ADDITION TO THE FOLLOWING PARTS FOR EACH OPTION

REF AC RMS SIGNAL CONDITIONING
0.1V OPTION (RAC06) P.C. ASSY
PL50-1090 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 1.0 µf, 50V	23-510001
C5	CAPACITOR, 10pf, 5%, DM10	23-310002
R1,3	RESISTOR SET, GROUP 20 200K (R1) ITEM 4 2 MEG (R3) ITEM 5	22-58-1012G20
Z1	I. C. OP. AMP., LF357	24-420357

REF AC RMS SIGNAL CONDITIONING
1.0V OPTION (RAC07) P.C. ASSY
PL50-1091 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 0.15µf, 400V, POLYCARB	23-510025
C2	CAPACITOR, 5pf, DM15	23-311000
C5	CAPACITOR, 10pf, 5%, DM10	23-310002
R1,3	RESISTOR SET, GROUP 20 2 MEG (R1) ITEM 1 2 MEG (R3) ITEM 5	22-58-1012G20
Z1	I. C. OP. AMP., LF356	24-420356

REF AC RMS SIGNAL CONDITIONING
100.0V OPTION (RAC09)
PL50-1093 REV.-

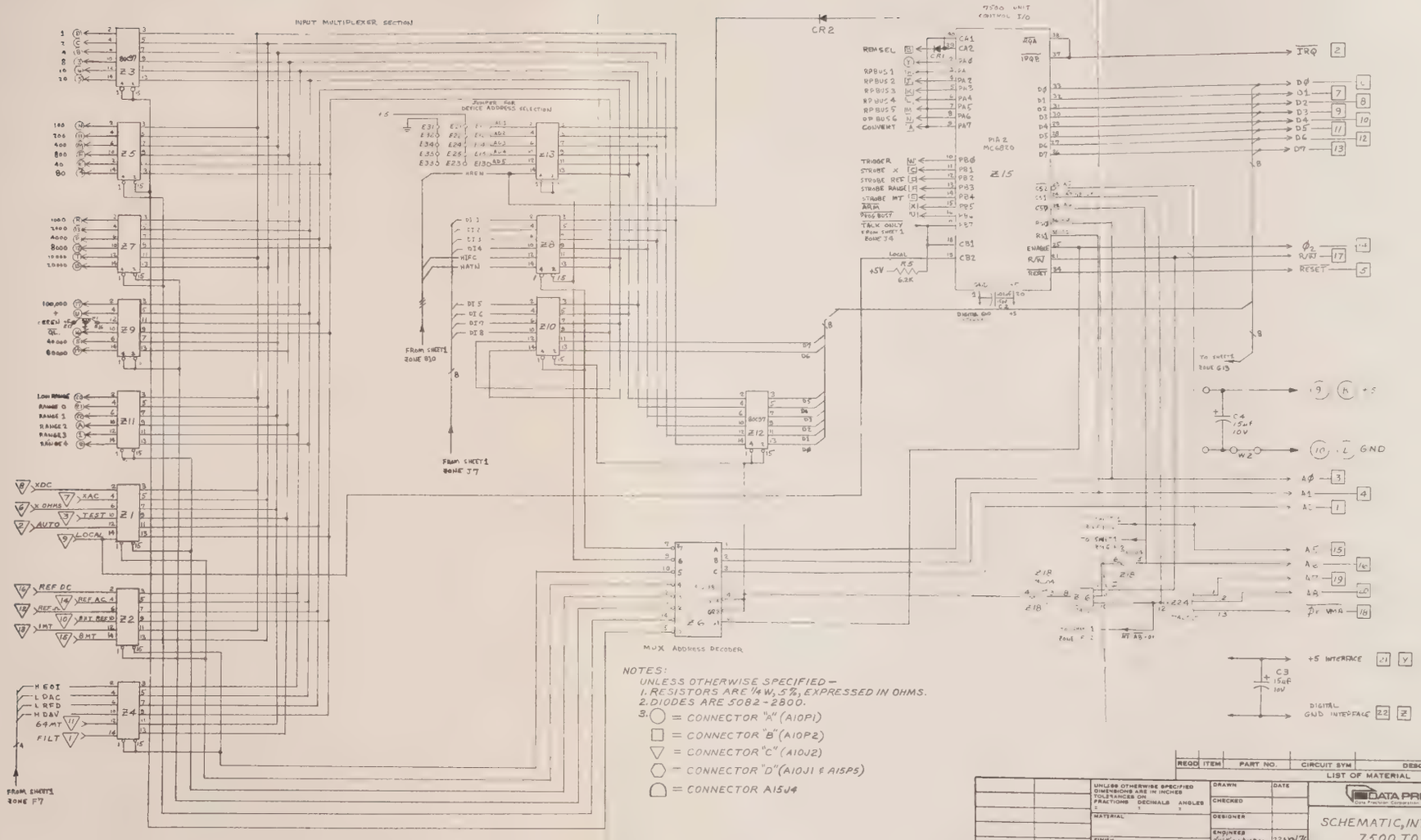
REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 0.15µf, 400V, POLYCARB	23-510025
C2	CAPACITOR, 5pf, DM15	23-311000
C6	CAPACITOR, 1000pf, DM15	23-311036
R1,3	RESISTOR SET, GROUP 20 2 MEG (R1) ITEM 1 20K (R3) ITEM 2	22-58-1012G20
Z1	I.C. OP. AMP., LF356	24-420356

REF AC RMS SIGNAL CONDITIONING
10.0V OPTION (RAC08)
PL50-1092 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 0.15µf, 400V, POLYCARB	23-510025
C2	CAPACITOR, 5pf, DM15	23-311000
C6	CAPACITOR, 100pf, 5%, DM15	23-311011
R1,3	RESISTOR SET,GROUP 20 2 MEG (R1) ITEM 1 200K (R3) ITEM 4	22-58-1012G20
Z1	I.C., OP. AMP., LF356	24-420356

REF AC RMS SIGNAL CONDITIONING
250.0V OPTION (RAC10)
PL50-1094 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 0.15µf, 400V, POLYCARB	23-510025
C2	CAPACITOR, 5pf, DM15	23-311000
C6	CAPACITOR, .01µf, 2%, 50V	23-510024
R1,3	RESISTOR SET, GROUP 20 2 MEG (R1) ITEM 1 2K (R3) ITEM 2	22-58-1012G20
Z1	I.C. OP. AMP., LF356	24-420356



NOTES:
UNLESS OTHERWISE SPECIFIED —
1. RESISTORS ARE 1/4 W, 5%, EXPRESSED IN OHMS.
2. DIODES ARE 5082-2800.
3. ○ = CONNECTOR "A" (A10P1)
□ = CONNECTOR "B" (A10P2)
▽ = CONNECTOR "C" (A10J2)
⬡ = CONNECTOR "D" (A10J1 & A15P5)
∩ = CONNECTOR A15J4

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

DRAWN DATE

CHECKED

DESIGNER

ENGINEER 12 NOV 76

APPROVED

RELEASED

WEIGHT

DATA PRECISION CORP

SCHEMATIC, INTERFACE, I/O SECTION
7500 TO STD 488 A10

CODE IDENT NO	SIZE	55-1020	REV
	D		A

SCALE ACCOUNT NO SHEET 2 OF 2

P.C. 50-1023 REV

NEXT ASSY USED ON

APPLICATION

NOTE: Sheet 1 of 2 (55-1020) See Page 9-28

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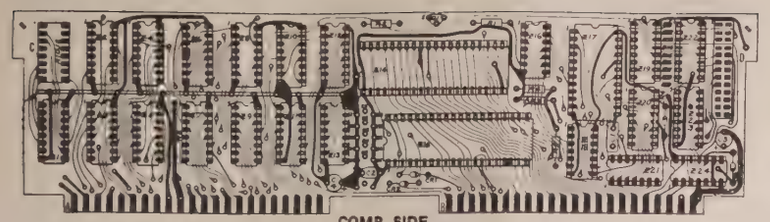
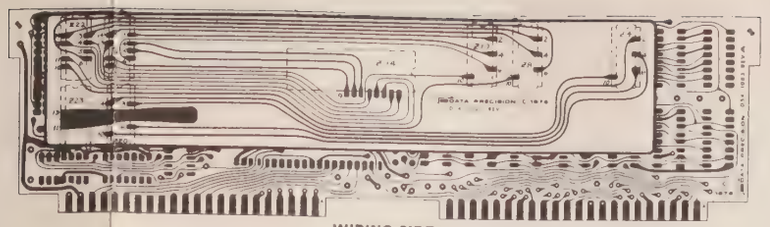


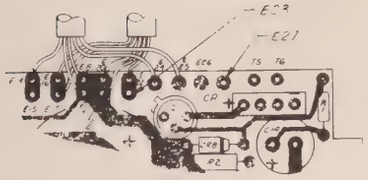
COMP. SIDE



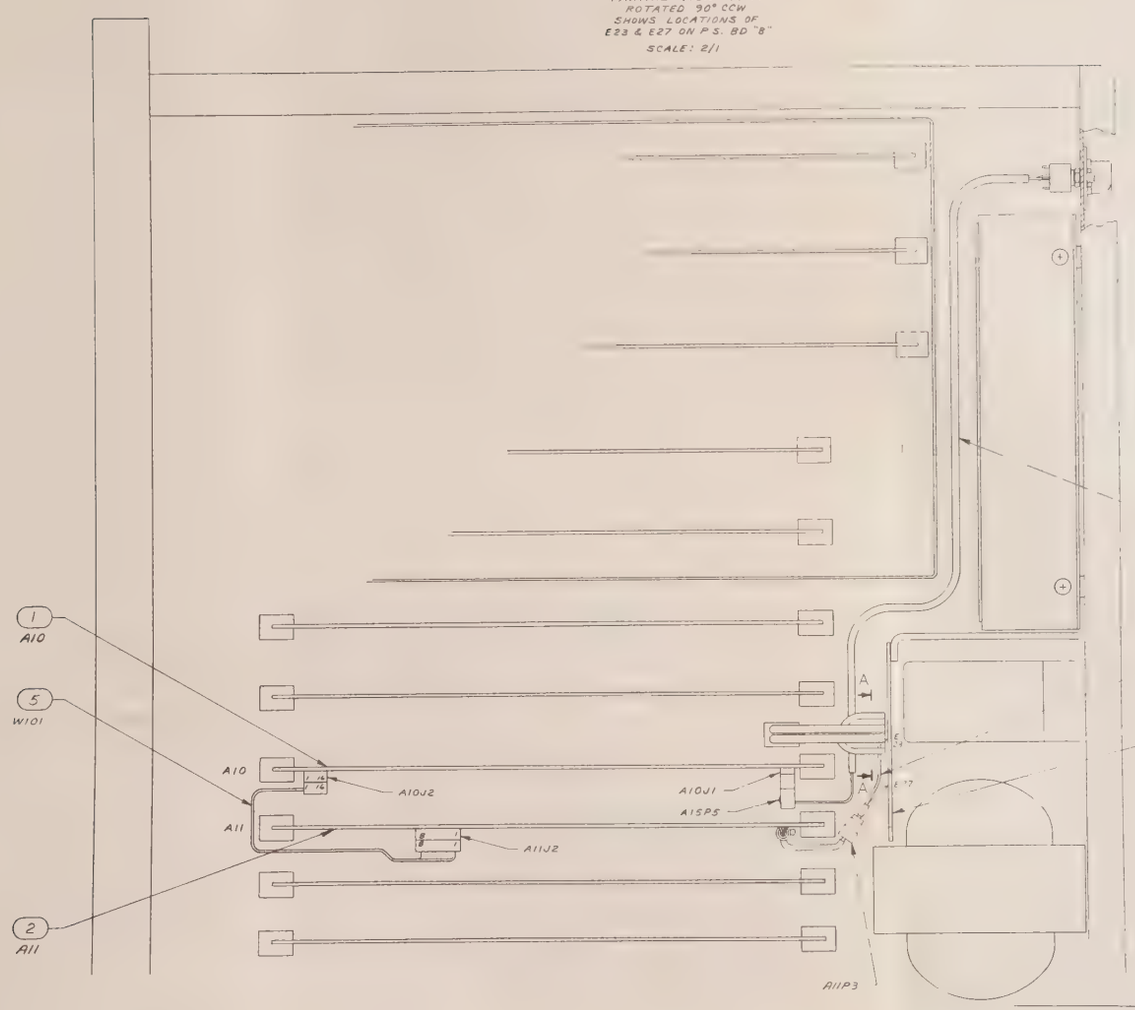
WIRING SIDE

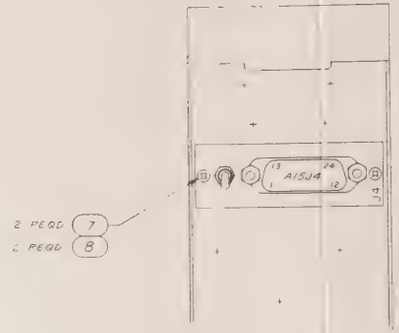
INTERFACE I/O SECTION, OPTION D10
7500 TO STD 488 P.C. ASSY (A10)
PL50-1083 REV. B

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1	CAPACITOR, 390pf, DM15	23-311026
C2	CAPACITOR, 0.01 µf, 150V	23-111006
C3,4	CAPACITOR, 15 µf, 10V	23-441003
CR1,2,3,4	DIODE,SCHOTTKY,5082-2800	24-110004
Q1	TRANSISTOR, 2N5818	24-235818
R1	RESISTOR, 1K, ¼W, 5%	22-021029
R2,3	RESISTOR, 20K, ¼W, 5%	22-022039
R4	RESISTOR, 10K, ¼W, 5%	22-021039
R5	RESISTOR, 6.2K, ¼W, 5%	22-026229
Z1 thru Z5	I.C., 80C97	24-G80C97
Z7 thru Z13		
Z6	I.C., 74LS138	24-E0LS138
Z11,15	I.C., MC6820	24-522000
Z16	I.C., 74LS11	24-E0LS11
Z17	I.C., 93L08	24-C93L08
Z18	I.C., 74LS04	24-E0LS04
Z19,20,22,23	I.C., MC3441	24-533000
Z21	I.C., 74LS02	24-E0LS02
Z24	I.C., 74LS27	24-E0LS27



PARTIAL VIEW A-A
ROTATED 90° CCW
SHOWS LOCATIONS OF
E23 & E27 ON P.S. BD "B"
SCALE: 2/1





WIRING CONNECTIONS		
FROM:	TO:	VIA ITEM NO
A15P6-RED	P.S. BD "B"-E23	4
A15P6-YEL	P.S BD "B"-E27	4
A10J2-#	A11J2-#	5

- PINS 1 THRU 16 ARE CORRESPONDING,
I.e. PIN 1 TO PIN 1, ETC.

NOTES:
1. SEE SEPARATE PARTS LIST PL50-1088
2. INSTALL JUMPERS ON A10 & A11 PER DWG. A55-1038.

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
7500
APPLICABLE SPECIFICATIONS
NEXT ASSY USED ON
APPLICATION

DRAWN jpc DATE 20CT76
CHECKED
DESIGNER
ENGINEER JC Langevin 20CT76
APPROVED
RELEASED
WEIGHT

DATA PRECISION CORP

INSTALLATION ASSEMBLY
INTERFACE, 7500 TO STD 488
OPTION D10

CODE IDENT NO 51692 | SIZE D | 57-1088 | REV A
SCALE 1/1 | ACCOUNT NO | SHEET 1 OF 1

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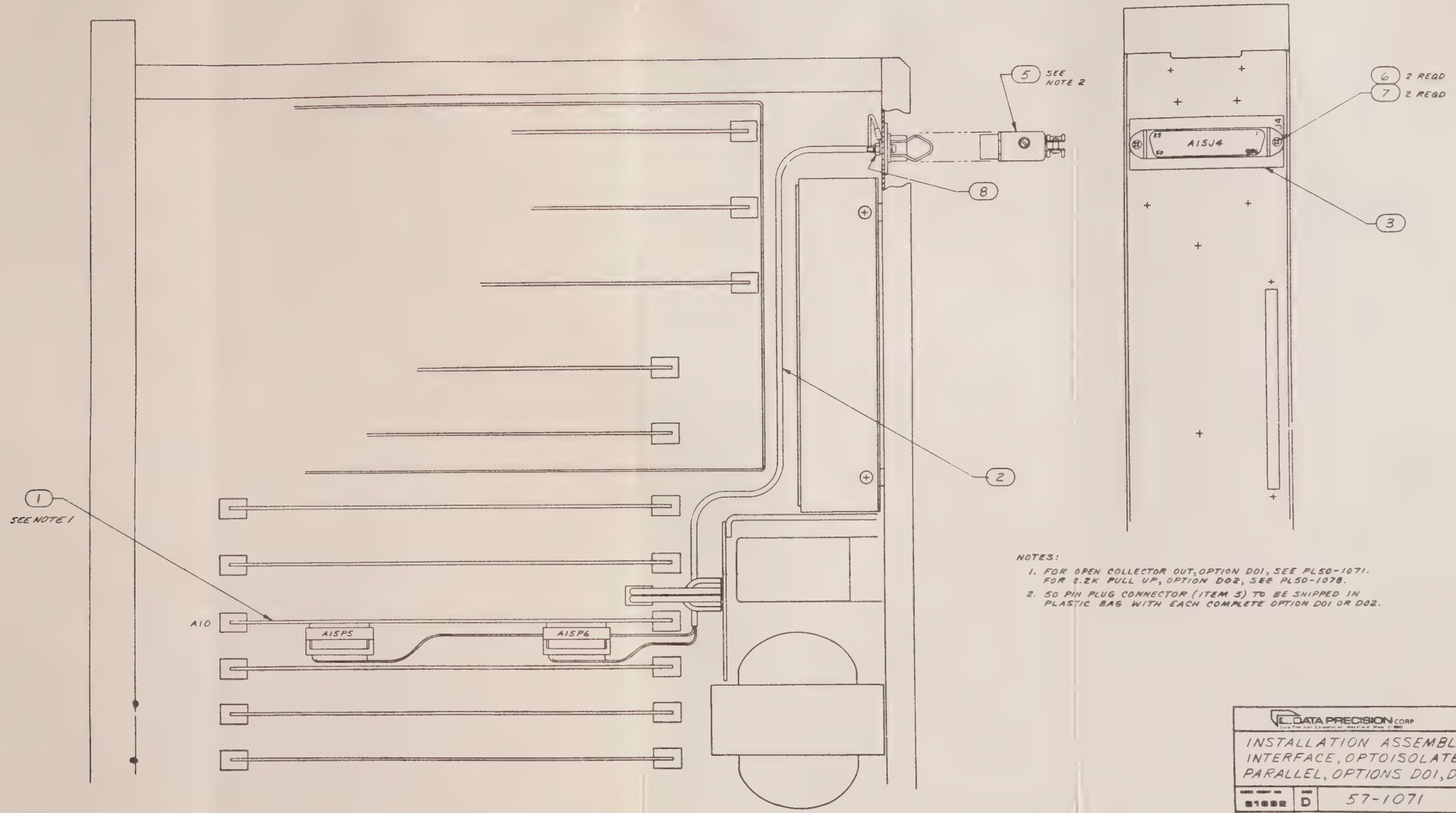

NOTES:

1. FOR OPEN COLLECTOR OUT, OPTION D01, SEE PL50-1071. FOR 2.2K PULL UP, OPTION D02, SEE PL50-1078.
2. 50 PIN PLUG CONNECTOR (ITEM 5) TO BE SHIPPED IN PLASTIC BAG WITH EACH COMPLETE OPTION D01 OR D02.

DATA PRECISION CORP

INSTALLATION ASSEMBLY INTERFACE, OPTOISOLATED, PARALLEL, OPTIONS D01, D02

51882	D	57-1071	A
SCALE 1/1	ACCOUNT NO	SHEET 1 OF 1	

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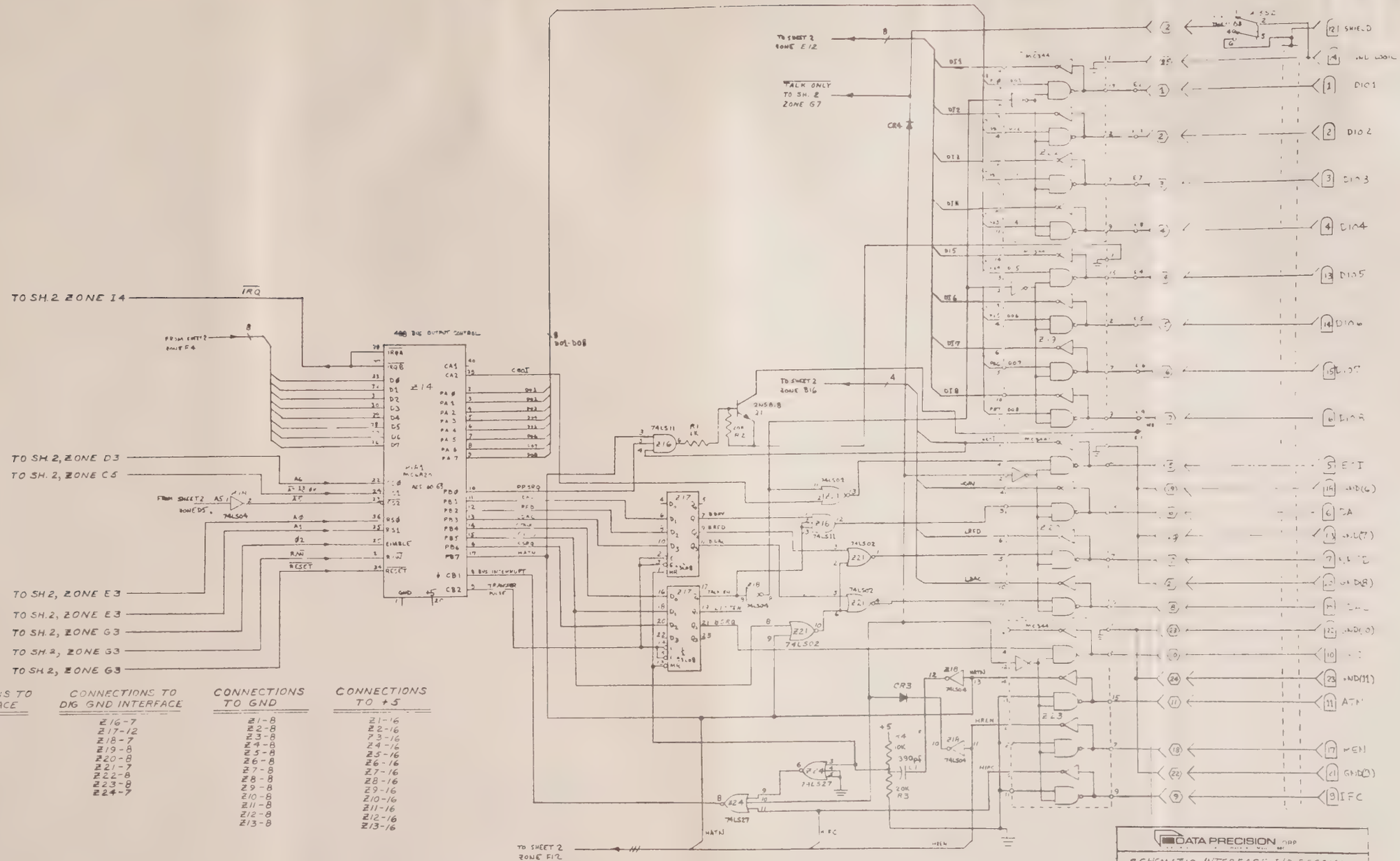

CONNECTIONS TO +5 INTERFACE	CONNECTIONS TO DIG GND INTERFACE	CONNECTIONS TO GND	CONNECTIONS TO +5
Z16-14	Z16-7	Z1-8	Z1-16
Z17-24	Z17-12	Z2-8	Z2-16
Z18-14	Z18-7	Z3-8	Z3-16
Z19-16	Z19-8	Z4-8	Z4-16
Z20-16	Z20-8	Z5-8	Z5-16
Z21-14	Z21-7	Z6-8	Z6-16
Z22-16	Z22-8	Z7-8	Z7-16
Z23-16	Z23-8	Z8-8	Z8-16
Z24-14	Z24-7	Z9-8	Z9-16
		Z10-8	Z10-16
		Z11-8	Z11-16
		Z12-8	Z12-16
		Z13-8	Z13-16

DATA PRECISION corp

SCHEMATIC, INTERFACE I/O SECTION
7500 TO STD 488 A10
(ANNOTATION ONLY)

CODE IDENT NO	SIZE D	55-1020	REV A
SCALE	ACCOUNT NO	SHEET 1 OF 2	

*NOTE: Sheet 2 of 2 (55-1020) See Page 9-25

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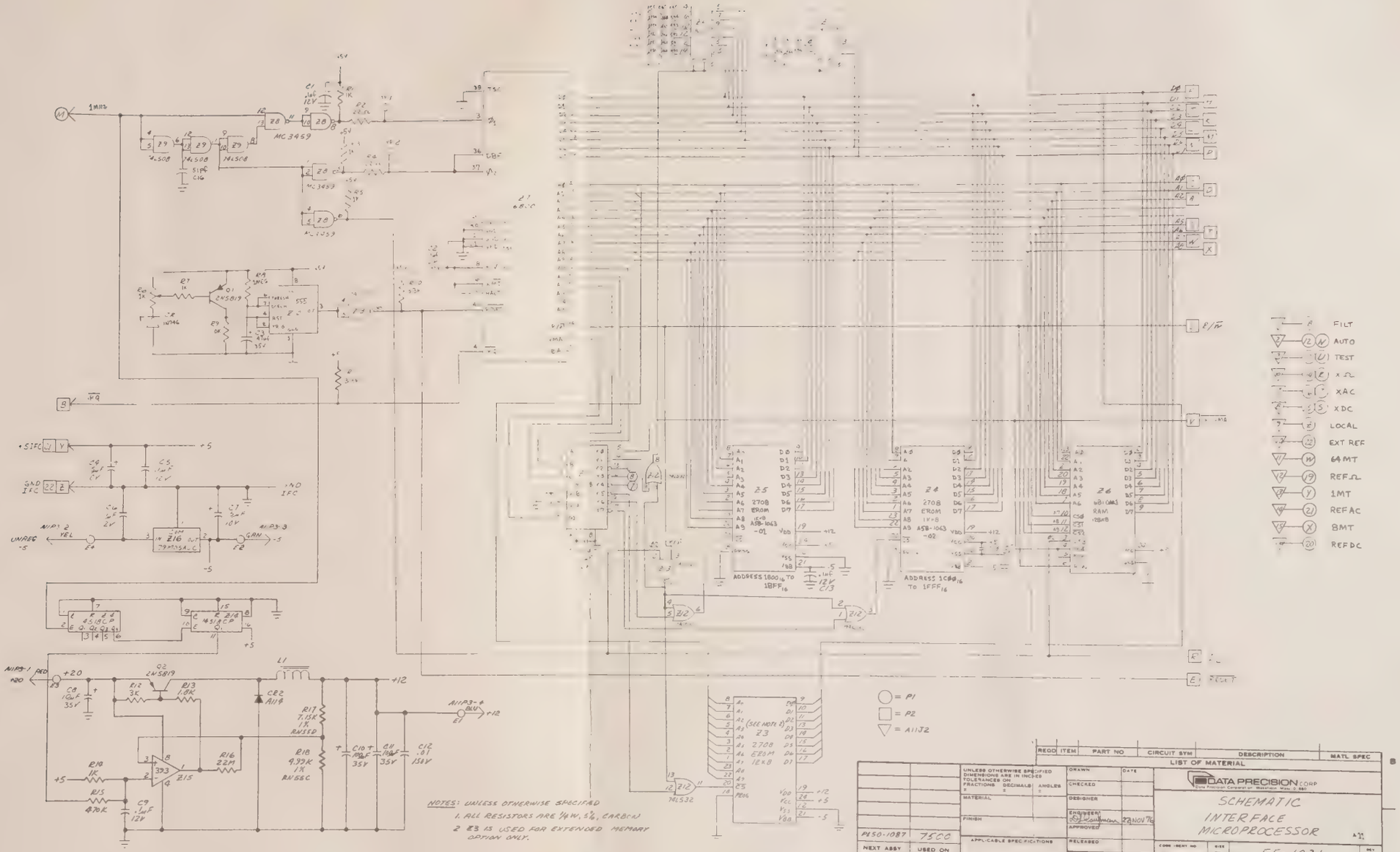

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

DATA PRECISION CORP

SCHEMATIC
INTERFACE
MICROPROCESSOR

P150-1087	7500		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

DRAWN — DATE

CHECKED

DESIGNER

ENGINEER — 22 NOV 76

APPROVED

RELEASED

WEIGHT

CODE IDENT NO	SIZE	DRAWING NO	REV
51892	D	55-1021	A

SCALE — ACCOUNT NO — SHEET 1 OF 1

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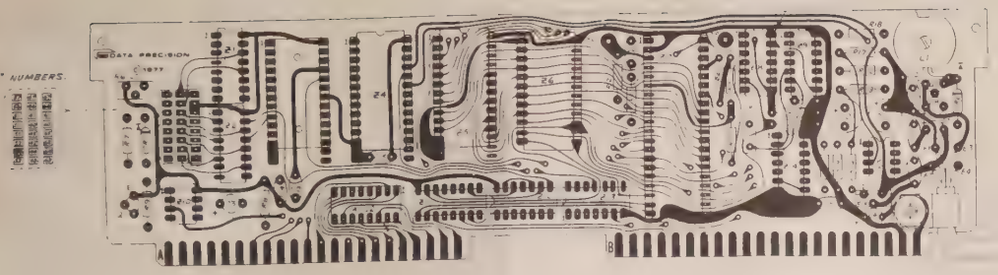
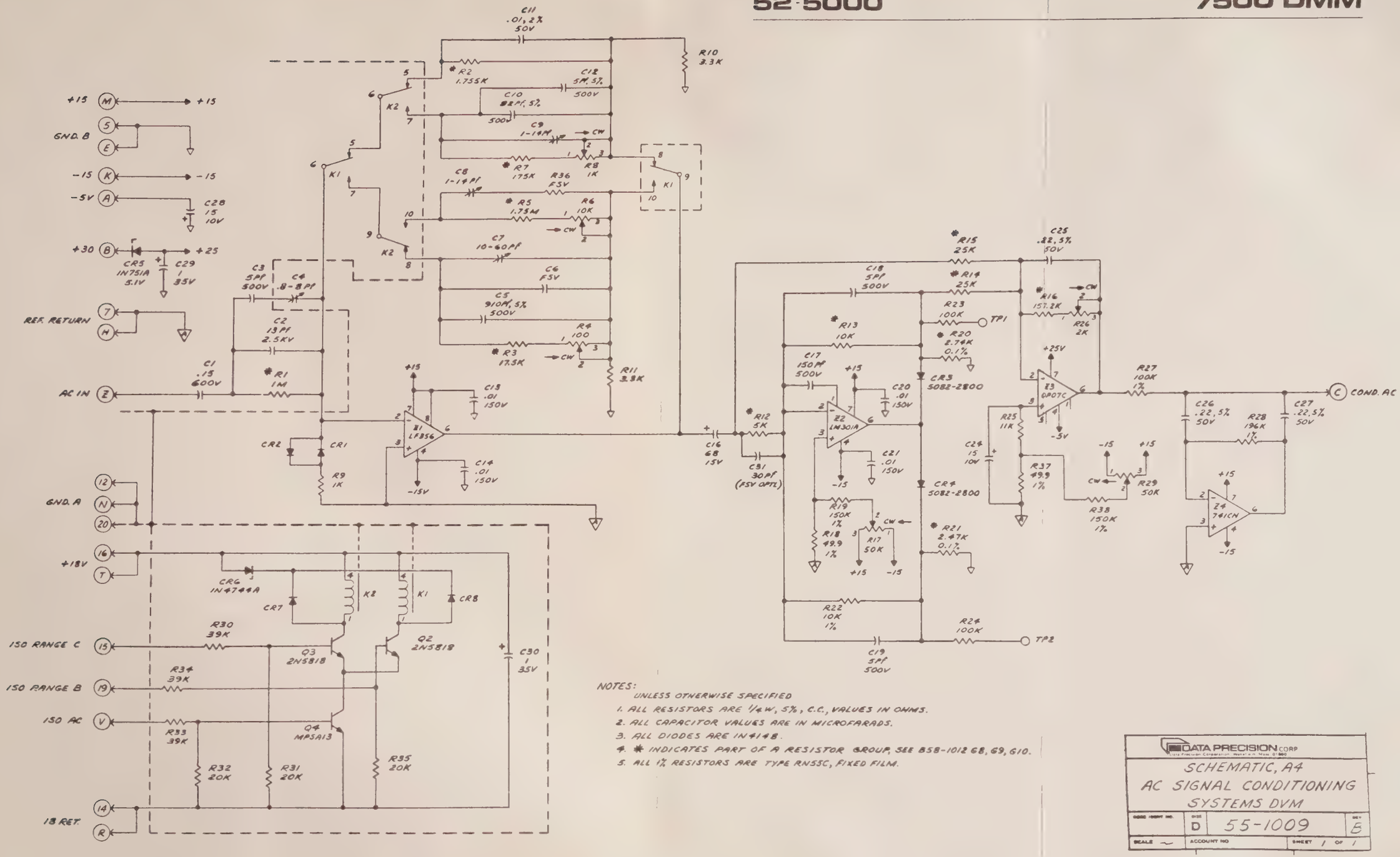


INTERFACE IMCROPROCESSOR P.C. ASSY
PL50-1087 REV. E

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
C1,2,5,6,9,13,14,15	CAPACITOR,DISC, .1μf, 12V, 20%	23-118206
C3	CAPACITOR,TANT, .47μf, 35V, 20%	23-441051
C4,7	CAPACITOR,TANT, 15μf, 10V, 20%	23-441003
C8	CAPACITOR,TANT, 10μf, 35V, 20%	23-441002
C10,11	CAPACITOR, AL. ELECTROLYTIC,100μf,35V	23-620002
C12	CAPACITOR,DISC, .01μf, 150V	23-111006
C16	CAPACITOR,MICA,51pf,DM15	23-311006
CR1	DIODE, 1N746A	24-120062
CR2	DIODE, A114A	24-100114
L1	INDUCTOR ASSY (C57-1099)	PL50-1099
Q1,2	TRANSISTOR, 2N5819	24-245819
R1,3,5,7,14	RESISTOR, 1K, ¼W, 5%	22-021029
R2,4	RESISTOR, 22Ω, ¼W, 5%	22-022209
R6	RESISTOR,TRIMMER, 1K	22-670102
R8	RESISTOR, 1MEG, ¼W, 5%	22-021059
R9	RESISTOR, 10K, ¼W, 5%	22-021039
R10,11	RESISTOR, 3.3K, ¼W, 5%	22-023329
R12	RESISTOR, 3K, ¼W, 5%	22-023029
R13	RESISTOR, 1.8K, ¼W, 5%	22-021829
R15	RESISTOR, 470K, ¼W, 5%	22-024749
R16	RESISTOR, 22MEG, ¼W, 5%	22-022269
R17	RESISTOR, 7.15K, 1%, RN55D	22-337151
R18	RESISTOR, 4.99K, 1%, RN55C	22-344991
Z1,2	I.C., MM80C97	24-G80C97
Z4	PROGRAMMED EROM(1024 x 8 Bit)	24-58-1063-02
Z5	PROGRAMMED EROM(1024 x 8 Bit)	24-58-1063-01
Z6	I.C., RAM6810	24-501000
Z7	I.C., MICROPROCESSOR 6800	24-521000
Z8	I.C., MC3459P	24-531000
Z9	I.C., SN74LS08	24-E0LS08
Z10	I.C., TIMER 555	24-400555
Z11	I.C., SN74LS138	24-E0LS138
Z12	I.C., SN74LS32	24-E0LS32
Z13	I.C., SN74LS00	24-E0LS00
Z14	I.C., MC14518CP	24-L14518
Z15	I.C., LM393	24-400393
Z16	VOLTAGE REGULATOR,79M05AVC	24-379M05



NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4 W, 5%, C.C., VALUES IN OHMS.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. ALL DIODES ARE IN4148.
4. * INDICATES PART OF A RESISTOR GROUP, SEE 858-1012 G8, G9, G10.
5. ALL 1% RESISTORS ARE TYPE RN55C, FIXED FILM.

DATA PRECISION CORP
SCHEMATIC, A4
AC SIGNAL CONDITIONING
SYSTEMS DVM
SIZE D 55-1009 REV E
SCALE — ACCOUNT NO SHEET 1 OF 1

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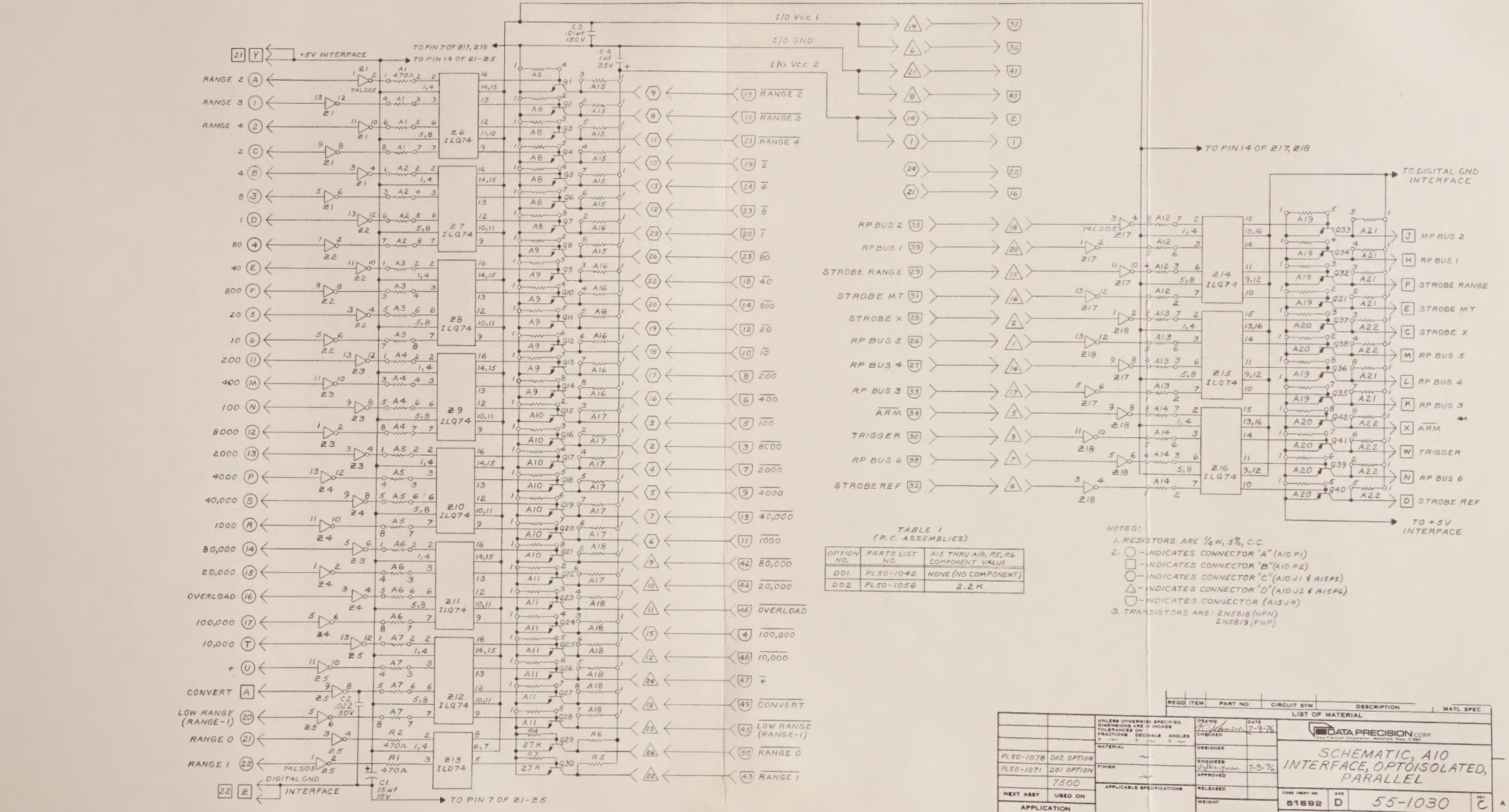

TABLE 1
(P.C. ASSEMBLIES)

OPTION NO.	PARTS LIST NO.	A15 THRU A18, R5, R6 COMPONENT VALUE
D01	PL50-1042	NONE (NO COMPONENT)
D02	PL50-1056	2.2K

NOTES:
1. RESISTORS ARE 1/4 W, 5%, C.C.
2. ○ - INDICATES CONNECTOR "A" (A10 P1)
   □ - INDICATES CONNECTOR "B" (A10 P2)
   ⬡ - INDICATES CONNECTOR "C" (A10 J1 & A15P5)
   △ - INDICATES CONNECTOR "D" (A10 J2 & A15P6)
   ▢ - INDICATES CONNECTOR (A15U4)
3. TRANSISTORS ARE: 2N5818 (NPN)
   2N5819 (PNP)

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC
				LIST OF MATERIAL	

PL50-1078	D02 OPTION
PL50-1071	D01 OPTION
7500	
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN — DATE 7-9-76
CHECKED
DESIGNER
ENGINEER — 7-9-76
APPROVED
RELEASED
WEIGHT

DATA PRECISION CORP.
Data Precision Corporation, Wakefield, Mass. 01880

SCHEMATIC, A10 INTERFACE, OPTOISOLATED, PARALLEL

CODE IDENT NO.	SIZE		REV
51692	D	55-1030	C
SCALE ~	ACCOUNT NO.	SHEET 1 OF 1	

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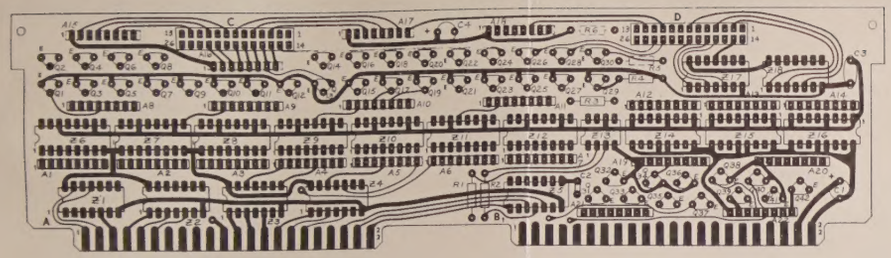

INTERFACE, OPTOISOLATED PARALLEL P.C. ASSY (BASIC) (D01)
PL50-1042 REV. A

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A1 thru A7		
A12,A13,A14	RESISTOR NETWORK, 470Ω	22-731003
A8,A9,A10,A11	RESISTOR NETWORK, 27K	22-730003
A19,A20	RESISTOR NETWORK, 2.2K	22-730001
A21,A22	RESISTOR NETWORK, 10K	22-730002
C1	CAPACITOR, 15μf, 10V	23-441003
C2	CAPACITOR, 0.022μf, 50V	23-140100
C3	CAPACITOR, 0.01μf, 150V	23-111006
C4	CAPACITOR, 1μf, 35V	23-441001
Q1 Thru Q30	TRANSISTOR, 2N5818	24-235818
Q31 Thru Q42	TRANSISTOR, 2N5819	24-245819
R1,2	RESISTOR, 470Ω, ¼W, 5%	22-024719
R3,4	RESISTOR, 27K, ¼W, 5%	22-022739
Z1 Thru Z5,17,18	I.C., 74LS05	24-E0LS05
Z6 Thru Z12, Z14,Z15,Z16	I.C., ILQ74	24-NILQ74
Z13	I.C., ILD74	24-NILD74

THE FOLLOWING OPTION USES THE BASIC P/L (PL50-1042 IN ADDITION TO THE FOLLOWING PARTS

INTERFACE, OPTOISOLATED PARALLEL 2.2K PULL UP OPTION (D02) P.C. ASSY
PL50-1056 REV.-

REFERENCE DESIGNATION	DESCRIPTION	D.P. PART NO.
A15 Thru A18	RESISTOR NETWORK, 2.2K	22-730001
R5,6	RESISTOR, 2.2K, ¼W, 5%	22-022229

MP MASTER
MA28740

DATA PRECISION
...years ahead

52-5000-A